High current welding diodes: Impact of silicon wafer thickness and diffusion profile on forward voltage drop

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Abstract

The welding diode design is analyzed using device simulations as well as electrical measurements to carry out an optimal technology from the performance point of view; especially low forward voltage drop, reproducibility of processing and high yield are desired. A new diffusion process is demonstrated as an enabler of superior electrical performance without necessity of aggressive wafer thinning.

1 Introduction

Welding diodes are designed for medium and high frequency welding equipment and optimized for high current rectifiers. The forward voltage drop must be very low, and the output current is high.

ABB provides both encapsulation types: encapsulated and housingless welding diodes, as shown on the figure below.

Fig. 1: ABB welding diodes in encapsulated (top) and housingless (bottom) design.

Increasing demand for resistive welding efficiency in automotive industry requires also a higher efficiency and reliability of welding diodes [1]. As the maximal average forward current I_{FAVM} can be found in the range of 6 to 14 kA depending on the operation frequency and package size, or even higher for aluminum welding [2], excellent diode forward characteristics are necessary for overall system efficiency.

2 Theory and device simulation

The welding diode forward characteristics are described by the forward voltage drop V_F, which is emerging at emitter junctions J_1 and J_2 and the middle (N^- base) region [3].

$$V_F = V_{J1} + V_{J2} + V_m \tag{1}$$

For the previously mentioned current load, which can reach up to 20 kA, we can express the voltage drop of the middle region V_m by following approximation

$$V_m \approx \left(\frac{W_m}{\mathrm{L}}\right)^2 \tag{2}$$

Where W_m is the width of the middle region at concentration 10^{18} cm^{-3} (see Fig. 2) and L is the diffusion length of excess carriers in the middle region. To lower the V_m, the term W_m/L should be relatively small, which means, that the middle region needs to be as thin as possible and, at the same time, the lifetime of carriers should be long enough, since the diffusion length is given by a well-known equation (as an example, let´s use the expression for diffusion length of the holes)

$$L_p = \sqrt{D_p \cdot \tau_p} \tag{3}$$

where D is the diffusion coefficient and τ is the carrier lifetime. This situation is quantitatively illustrated by a device simulation shown below.

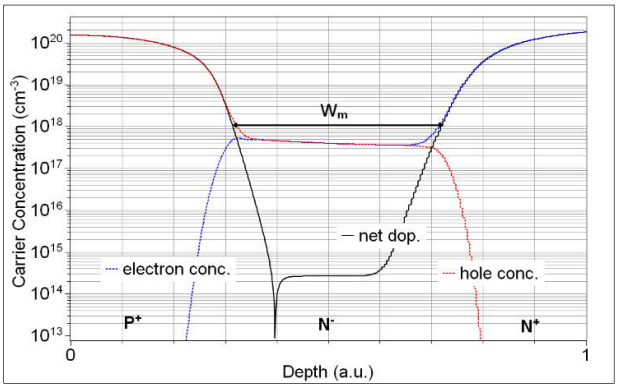

Fig. 2: Doping profile and free carrier concentration in the forward direction for 20 kA at 170°C.

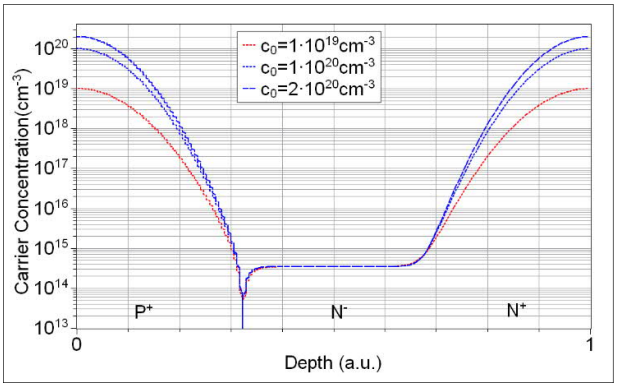

Fig. 3: Simulation of different surface concentrations c_0 of the emitters.

From the simulation above we can see, that the biggest impact on the V_m has the width of the middle region W_m, where the carrier concentration typically reaches the level of 10^{18} cm^{-3}. Throughout this paper, when talking about the parameter W_m, we therefore consider the level of 10^{18} cm^{-3}, unless otherwise stated.

We have the following options to reduce the V_m:

A. Use thinner silicon wafer,
B. Use longer diffusion time of dopants,
C. Increase excess carrier lifetime.

However, as the middle region of this low voltage diode is short relatively to the whole wafer thickness, one cannot neglect the voltage drop of the emitters. This is illustrated in Fig. 4, which shows the impact of the emitter surface concentration (simulation outcome in Fig. 3) on the voltage drop for a given width W_m.

Fig. 4 implies, that for reasonably low V_F, we need to achieve higher emitter surface concentration than 10^{20} cm^{-3}. This fact is important for the selection of diffusion species and methods used in processing.

The currently available cost-efficient diffusion methods giving the highest surface doping concentration usually do not provide the highest possible carrier lifetime (factor C above). When using the methods giving the highest lifetime, one must compromise the surface doping concentration. Such approach is demonstrated further in this paper.

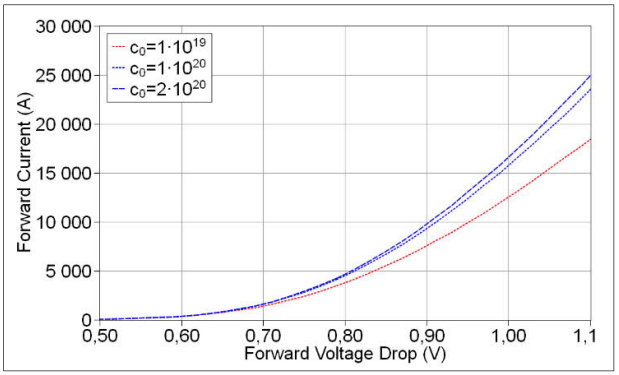

Fig. 4: Impact of the emitter surface concentration c_0 on the forward voltage drop simulated at 170°C.

2.1 Impact of wafer thickness

The doping profiles were simulated using the process simulator Athena from Silvaco [4] with default settings. The simulation has been performed for several wafer thicknesses, namely 170, 200 and 230 µm as can be seen in Fig. 5. The minimal N^- base width of 30 µm has been chosen with the intention not to affect the breakdown voltage of 400 V.

The goal is to estimate the impact of wafer thickness on the forward voltage drop V_F, considering the fact, that the overall forward voltage drop is given by the wafer thickness (factor A above) in combination with manufacturing technology (factors B and C).

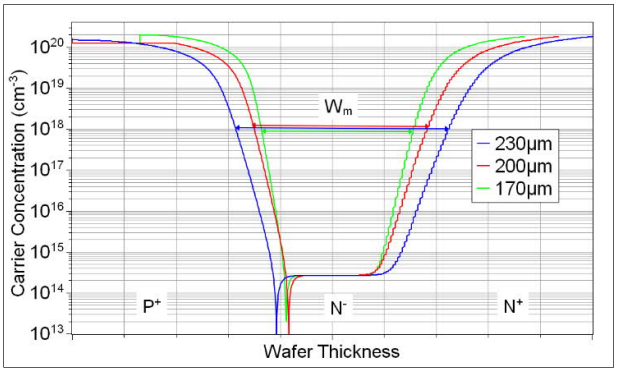

Fig. 5: Simulated doping profile for 170, 200 and 230 µm wafer thicknesses.

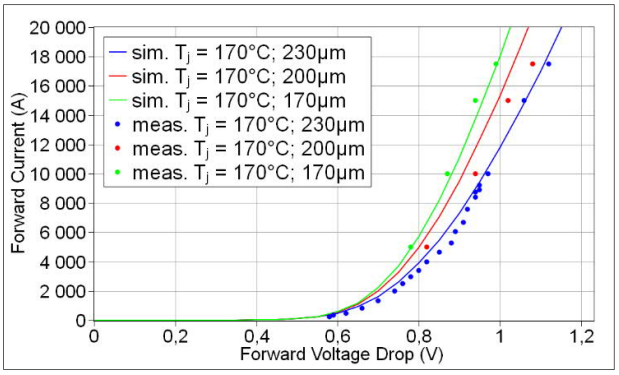

Fig. 6: Simulated and measured forward I-V curves at 170°C for silicon wafer thicknesses according to the previous figure.

The correctness of simulated diffusion profiles, resulting in the simulated forward characteristic, has been confirmed by experiments for the temperature of 170°C. The diodes were produced using our current technology. The impact of the wafer thickness is obvious. The thinner the silicon wafer, the lower the forward voltage drop. However, processing of too thin wafers increases demands on wafer handling and might negatively impact the production yield not only of high temperature diffusion processes, which are necessary for the high surface doping concentration discussed above, but also of the subsequent processes of the production flow. The usage of a thicker silicon wafer for smooth production would be possible, if the surface concentration of the emitters increased, for example by using another diffusion technology. The result of such effort is demonstrated next.

2.2 Diffusion process optimization

Based on the principles of semiconductor physics and our long-term practical experience with diffusion processes, a new diffusion process has been developed. It provides the following improvements:

- Excess carrier lifetime increased about half order of magnitude as verified by the Open Circuit Voltage Decay (OCVD) measurement, as demonstrated in Fig. 7 below,
- The emitter surface concentration at the level of 10^{20} cm^{-3} or higher as verified by spreading resistance measurements, and
- Reduction of the crossing point current of cold and hot I-V curves, which has a positive impact on the device reliability.

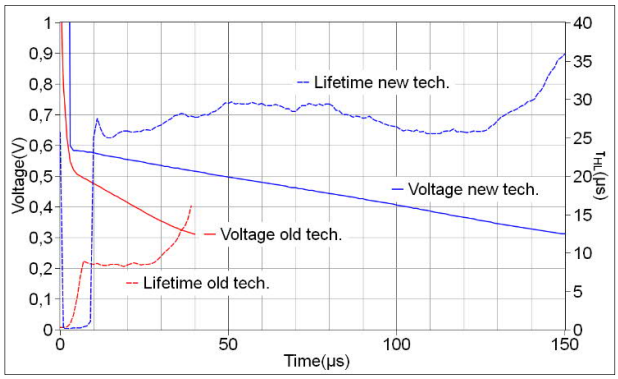

Fig. 7: OCVD measurement of diodes produced by the old and new technology.

The measured OCVD response [5] in Fig. 7 is re-calculated to the high-level carrier lifetime τ_{HL} according to the equation derived in the ref. [6]:

$$\tau_{HL} = -\frac{2 \cdot kT}{e}\left(\frac{dV}{dt}\right)^{-1} \qquad (4)$$

where dV/dt is the slope of the voltage decay. In agreement with ref. [7], the magnitude of the lifetime τ_{HL} is read-out from the graph at the position, where it makes sense from the physics point of view. For the new technology, it is for the time between 50 and 80 µs hereby giving the τ_{HL} = 28 µs, while for the old one, we subtract the τ_{HL} between the time 10 and 25 µs, giving τ_{HL} = 7 µs. The factor $\tau_{HL\ new}$ / $\tau_{HL\ old}$ = 3.5 between the new and the old technology characterizes the improvement in cleanliness achieved in the new process.

The resulting forward characteristics in Fig. 8 clearly show an improvement relative to the existing technology. As a result, the forward voltage drop has been reduced by 100 mV at 20 kA, whilst the wafer thickness has been kept at conservative level for high production yield. The reproducibility in volume production has been improved as well.

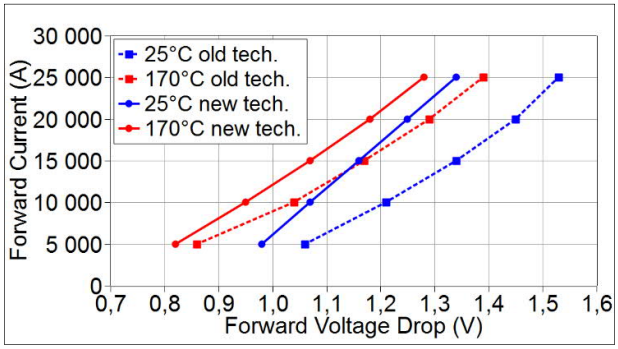

Fig. 8: I-V curves measured at 25 and 170°C of a diode prepared by the old and the new technology.

3 Conclusion

The impact of silicon wafer thickness, doping profile and carrier lifetime on the forward characteristics of high current welding diodes has been analyzed. Improved forward ratings were experimentally demonstrated based on improved diffusion process relative to standard high temperature processes. The usage of a conservative wafer thickness provides a stable and well reproducible technology.

4 Acknowledgement

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5 References:

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