TOBIAS WIKSTRÖM, CHRISTIAN WINTER – HITACHI ABB POWER GRIDS, SEMICONDUCTORS, SWITZERLAND

New IGCT platform for offshore wind converters exceeding 15 MW

Offshore wind generation will become a significant contributor in the global effort to decarbonize energy production. Higher-power wind turbines are an important trend in the wind industry, as they help to improve profitability. Today, the current generation of Hitachi ABB Power Grids IGCTs are part of the largest offshore wind converters, delivering in excess of 10 MW of power.

Medium voltage converters offer the clear advantages of smaller currents, low part counts, simpler installation, and reduced space and weight of the equipment. IGCT technology improves the efficiency and reliability of the wind converter significantly, enabling operators of medium voltage converters to reach the lowest Levelized Cost of Energy (LCOE) and highest return on capital.

Hitachi ABB Power Grids has developed an asymmetric 4.5kV IGCT platform to support the trend towards higher power output. This paper describes the new 6500 A, 4500 V Integrated Gate Commutated Thyristor (IGCT) designed for wind converters delivering 15 MW and above. The segment layout was developed with the goal of maximizing the controllable current, and tested layouts are fully described. The mechanical design is based on an existing platform for outer-ring-gate, 94 mm-diameter silicon wafers. The best layout variant reliably switches currents exceeding 8000 A at 2800 V in single pulse at high temperatures and frequency operation is stable up to a virtual junction temperature of approximately 230 °C.

The IGCT

The IGCT is, in principle, a thyristor-based device that, since its evolution from the Gate turn-off Thyristor (GTO) in the mid-1990s, established itself as the device of choice for medium voltage wind converters, industrial Medium Voltage Drives (MVD) and many other systems such as STATCOMs and interties. Thanks to the integration with a low-inductive gate unit, this device conducts like a thyristor (low on-state losses) and turns off like a transistor.

Today, IGCTs have been optimized for CSI and VSI applications with voltage ratings ranging from 4.5kV up to 10 kV, and are available as asymmetric, reverse blocking, and reverse conducting devices. For VSI topologies, the asymmetric IGCT has the highest power level for a given wafer size. In contrast, reverse conducting IGCTs with their monolithically integrated free-wheeling diodes offer more compact system assemblies. The gate unit and its connection to the power device is critical for switching performance which is normally delivered as an integral part of the IGCT. This ensures the necessary low-impedance connection and enables the manufacturer to take full ownership of the quality, ratings and applicability of the assembly. The hermetic press-pack design of the switch itself has years of proven reliability in the field, particularly regarding the power semiconductor device protection and load cycling capability.

Device architecture

The goal of this project was to use the lower thermal impedance and increased active area of the 94 mm wafer platform instead of the 91 mm platform that has been in production for more than twenty years. The 94 mm platform was first developed for an RC-IGCT for STATCOM applications [1] in 2014 - 2016.

The 94- and 91 mm housing platforms are identical on the outside; they differ only internally. The 91 mm wafer has its gate connection placed at around half of the device radius. Connecting the gate potential to the wafer from the radial outside inevitably means leading it through the cathode pole-piece that constitutes the principal electrode and thermal contact on the cathode side. The gate vias introduce obstructions in both the electrical and thermal circuits of the 91 mm device. In contrast, the gate contact of the 94 mm wafer is placed outside the device active area, which eliminates the obstructions in the cathode contact and decreases the thermal resistance. The space allocated for device active area is also improved, beyond the mathematical area increase of 6 - 7 % that results from changing the laser cut diameter from 91 to 94 mm. A more effective design, together with improved production precision that reduces required tolerances, allow an increase of the active GCT area from 42 to 51.4 cm^2, an increase of 22 %.

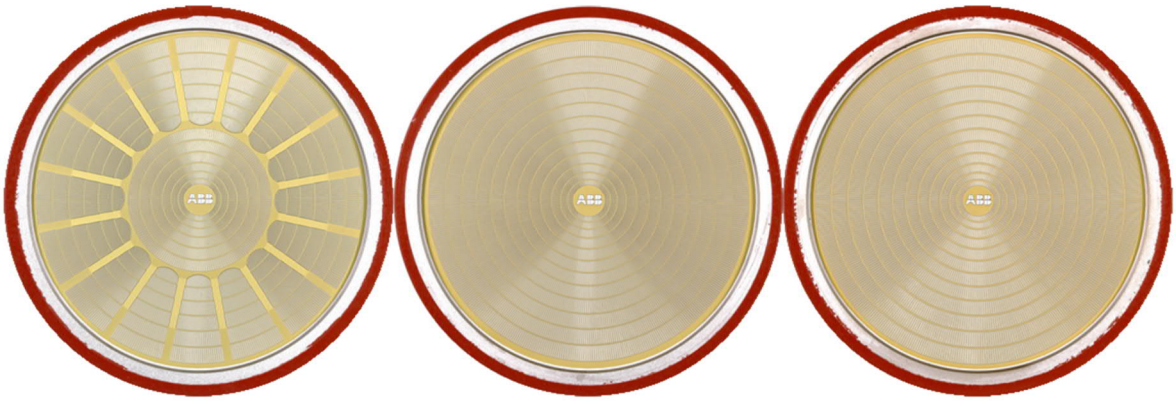

Fig. 1: Pictures of experimental wafer layouts investigated. All wafers are cut to 94 mm diameter. Left: HWY layout. Centre: VSW layout. Right: CSW layout

Segment layout experiment

Uncertainty around how the outer ring gate would influence the current controllability and gate metallization robustness of an asymmetric device, led to extensive simulation (the simulation method is described in [2]) of the impedance characteristics of the gate metallization of such devices. The simulations sparked an experiment investigating three design approaches to segment placement. An early simulation result showed that the layout has very little influence on the inductive impedance distribution over the wafer. The experiment therefore focused on the resistive properties. Figure 1 shows photographs of the initial three designs. All three designs are made up of twelve segment rings that contain a varying number of identical segments.

The rightmost photograph shows a variation of a conventional IGCT wafer layout, named ”Constant Segment Width” (CSW). As the name suggests, the segment width does not vary with placement radius and is equal to 250 µm.

The center photograph shows a further refinement of the conventional layout named ”Variable Segment Width” (VSW). For this layout variant, the segment width varies with radial placement on the wafer. The aim of the VSW concept is to help the innermost segments turn off faster, to counteract their disadvantageous position in relation to the gate contact, by making them narrower. This design attempts to compensate for the inherent speed disadvantage caused by the later arrival of the gate signal.

A third variant is shown in the leftmost photograph and is named ”Highway” (HWY). It is an attempt to avoid loading the approximate outer half of the segment rings with the current generated by the inner half. The HWY concept also features variable segment width, but the distribution is squeezed together in each of the inner- and outer segment ring compartments. The HWY layout allows for a wide range of additional trials: for example, where the gate metal of the two compartments is connected (if at all). The wafer in the photograph has its inner- and outer compartments re-connected after ring ten, but this can be hard to make out by the untrained eye. A further HWY variant that was investigated made the gate metallization thicker in the highways (or runners) that connect the inner compartment with the gate contact than in the compartments where the segments are placed. This is achieved by allowing the contact force buffer metal layer that is normally placed exclusively on top of the cathode segments also in the highway-region of the gate metallization. It gives a significant, up to a factor of two, increase of the highway metal height. The approach has disadvantages for other aspects of device robustness and would require additional testing before production-ready, but it is a fast and convenient way to modulate the sheet resistance of the highway metal layer in order to observe eventual effects on controllable current.

All three layout variants were manufactured with different gate metal layer thickness between one and two times the conventional thickness, to decrease the radial ohmic impedance of the gate metal layer. Physical IGCT segment layouts can be quite accurately described by the segment width and spacing distributions over the wafer. The details of the layout variants that were investigated are shown in graphs plotted in figure 2. The graphs show how the segment width (left graph) and segment-to-segment spacing (right graph) vary with segment-ring-center-radius over the wafer.

In addition to the maximum controllable current, the segment layout influences the ruggedness of the cathode contact, i.e. the on top of the segments. The impact is essentially defined by the ratio between anode pressed metal area and segment pressed metal area. As the segment packing density increases, the ratio also improves. The same factors also influence the power loss efficiency, albeit to an extent that is bordering on insignificant within reasonably applied design-parameter-sets.

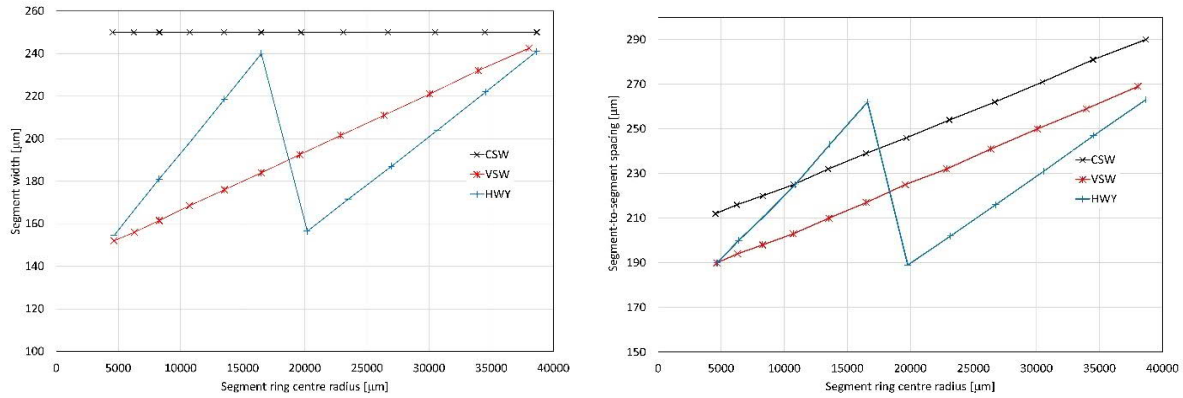

Fig. 2: Details of the segment layout of the three investigated designs: segment width distribution (left) and segment-to-segment spacing distribution (right).

Results

Power loss trade-off

As a consequence of the slightly different segment packing densities, the variants also display a small variation in the trade-off between static and dynamic losses. The trade-off between on-state voltage and turn-off losses for a few design variants are plotted in the graph in figure 3.

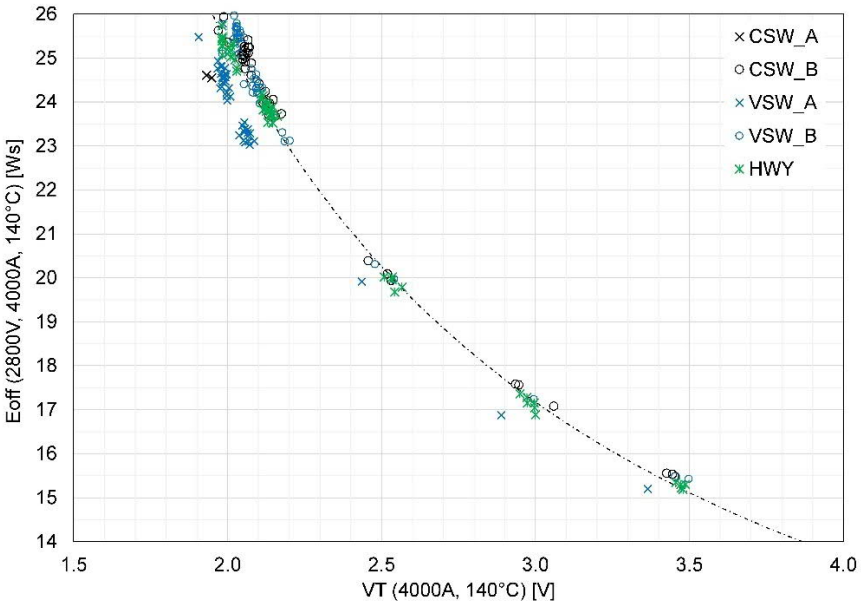

Fig. 3: Technology curve at 4000 A, 2800 V and Tj 140 °C

Maximal controllable current

All variants were tested to destruction in single pulse mode, at junction temperatures ranging from 25 °C to 160 °C. The current controllability distributions of the three main experimental groups at V_{DC} = 2800 V and T_j = 140 °C is shown on the right hand side of figure 4. The VSW layout clearly features the highest robustness and, somewhat unexpectedly because the simulations promised a better result, HWY the lowest.

A sample waveform of one of the highest switched currents, 8000 A, is plotted in figure 5. At low junction temperatures, however, there is a clear performance limit due to inductive voltage peaks. The over-voltage transients, which are a result of the energy stored in the stray impedance and the rapid current transients, push close to, or above, the avalanche capability of the device. At low temperatures, this happens at far lower currents than the device would be able to turn off, were it not for the over-voltage. In figure 6, a turn-off waveform at 25 °C, 6800 A and 2800 V is shown, illustrating this effect. To some extent, the device can clamp the voltage by generating avalanche current - the plateau at the maximal voltage - but if the energy stored in the stray impedance is too high this condition will cause the device to fail.

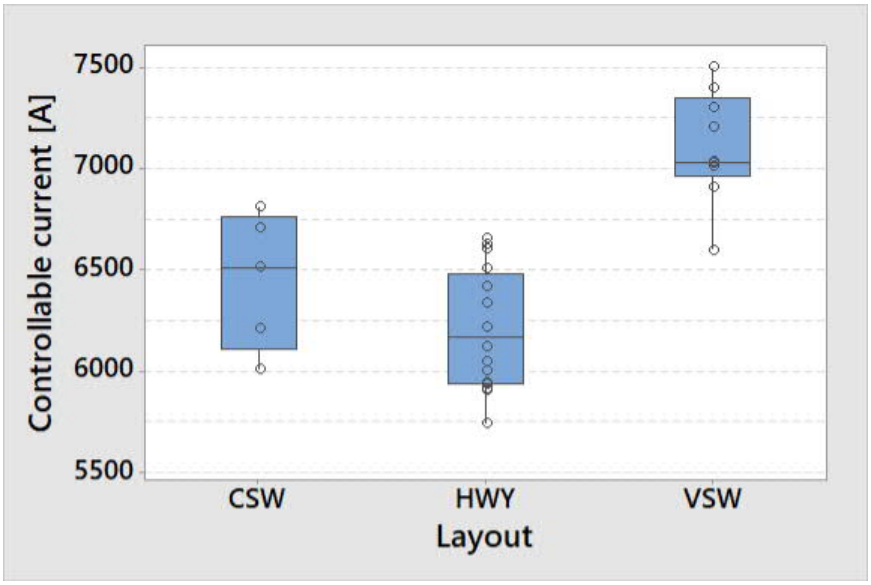

Fig. 4: A boxplot showing the distribution of maximal controllable current as tested over the three main layout variants.

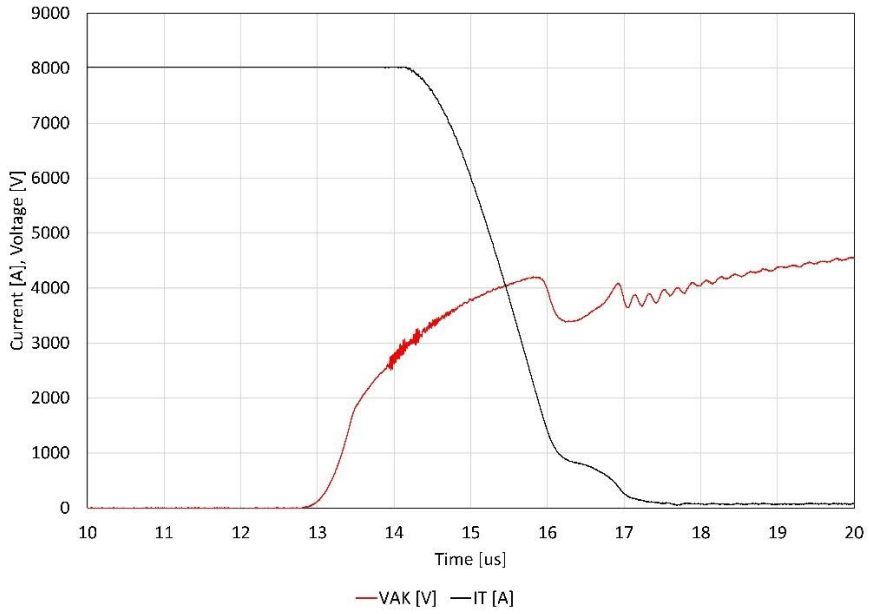

Fig. 5: A waveform showing one of the events with the highest switched current at T_j = 140 °C, I_T = 8000 A, V_{DC} = 2800 V.

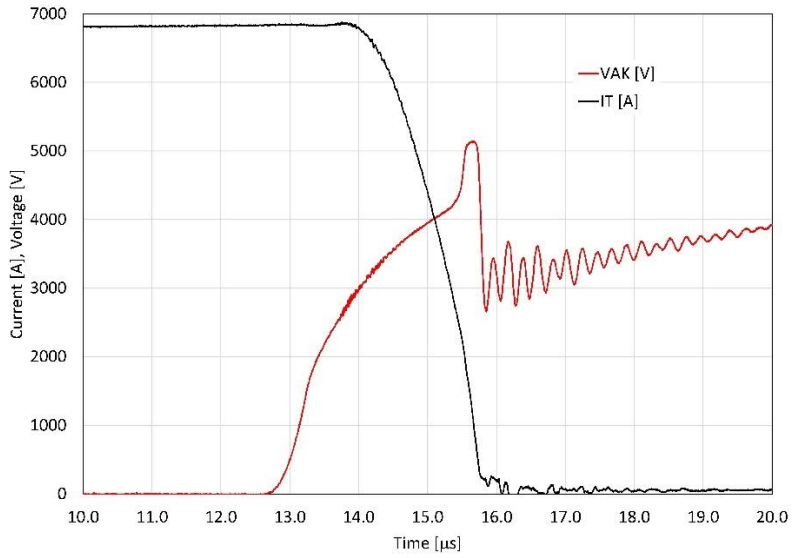

Fig. 6: Turn-off waveform at 25 °C, 6800 A, 2800 V_{DC}, illustrating the inductive voltage overshoot that exceeds the avalanche capability of the device. The stray impedance used for these measurements amounted to 325 nH.

Ruggedness at elevated temperature and frequency operation

Both frequency and HTRB testing demonstrated for the device is capable of supporting a $T_{vj,max}$ significantly above the required 140 °C. The frequency test uses a current chopper setup that allows the switching frequency, current, voltage and duty-cycle to be changed. Thermal failures were provoked at 100 Hz, 4850 A and 2800 V with a 95% duty cycle. The power losses under such conditions and thermal impedance of the cooling system allowed the junction temperature (T_{vj}) to be calculated as approximately 230 °C. A new frequency-test-facility was built to facilitate frequency testing above the rated current, and in very recent results, devices were tested up to 7000 A in frequencies up to 500 Hz without failure, a result that leaves little doubt about the robustness of this device for the future.

References

[1] M. Alexandrova and T. Wikström, “A Technology Platform for Reverse-Conducting Integrated Gate Commutated Thyristors with 94 mm Device Diameter”, in Proceedings of the PCIM, 2017, pp. 806–810.

[2] T. Wikström, T. Stiasny, M. Rahimo, D. Cottet, and P. Streit, “The Corrugated P-Base IGCT – a New Benchmark for Large Area SOA Scaling”, in Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs, 2007, pp. 39–32.