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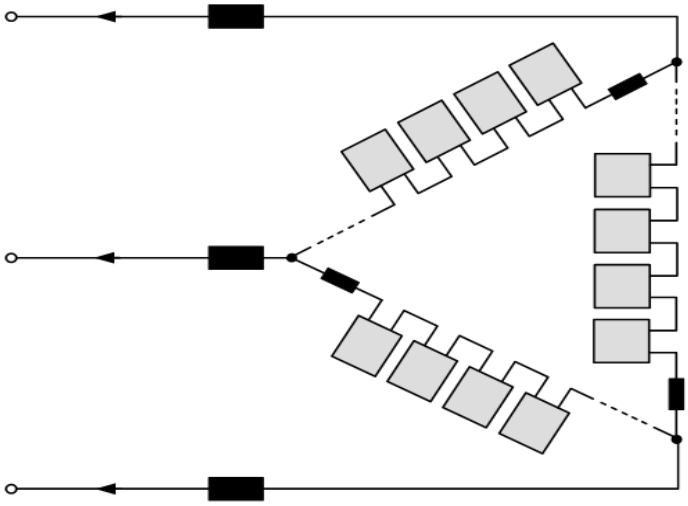
Sacrificial Bypass Thyristor for MMC applications

Modular multilevel converter topologies (MMC) in figure 1 must provide serial redundancy, reliably discharge a cell's energy storage and short its terminals in the event of a fault. The stored energy in some high-power applications is large enough to compromise the installation due to the risk of semiconductor housing rupture, external arcing, capacitor explosion or electro-mechanical rupture of electrical connections. In many power systems, semiconductor explosions are accepted in fault cases because they cannot be avoided. Instead, explosions are contained, and the cell terminals are shorted using a mechanical switch, items that all add to the system cost. This paper details a semiconductor design that increases the rupture limit for a bypass device to extreme levels. As a result, explosion-management cost is avoided. Further information about system ruggedness considerations can be found in [1], [2].



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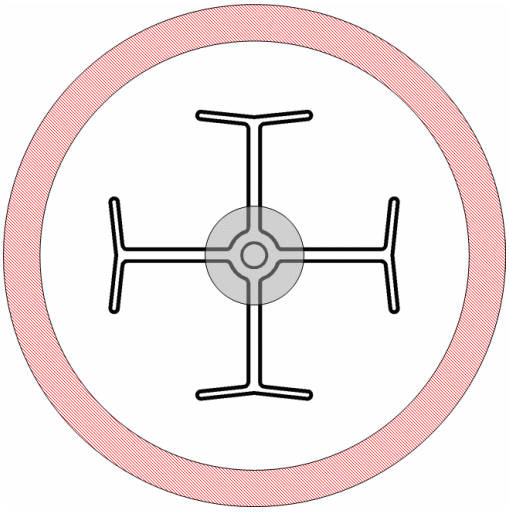
01 Intended MMC application



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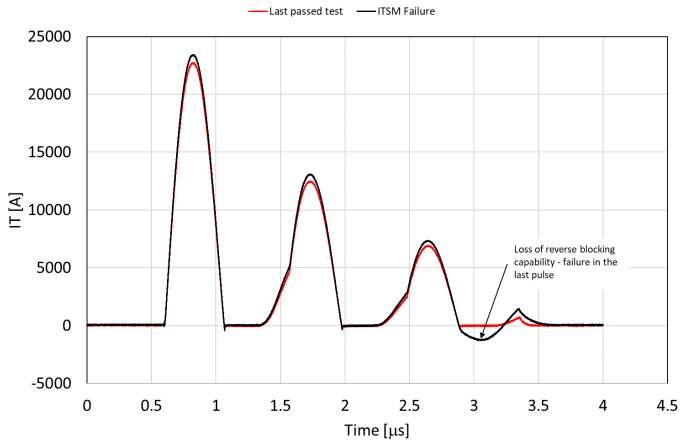
02 Wafer design with localized electron irradiation (masked)

Non-rupture criterion
Thyristor housing rupture is a concept standardized by the IEC [2], and this paper follows that standard as closely as possible. An important deviation is that the housing technology for containing an unmitigated edge arc at the targeted energy levels does not yet exist, assuming a reasonably sized device.

Design and performance - Wafer design
The wafer design is straightforward and based on an existing thyristor wafer type. There are two challenges for the wafer: limiting the maximal surge-current capability to an acceptable level and steering faults away from the wafer edge. The first challenge was met, while catastrophic edge faults could be mitigated by trigger assistance. This requires a quick enough turn-on command response to any fault, of course including edge faults, to turn on centrally before the current in an edge arc has risen to explosion levels. The approach taken was to constrict the current to a small central portion of the wafer using a high-dose electron irradiation of the rest of the active area, as shown in figure 2.

The on-state voltage increased to around 3 V at 100 A after irradiation. Irradiation led to a reasonably low maximal I_{TSM} capability for that wafer size, required for safe shorting of faulty cells without fully charged capacitors. Operation with an approximate 23 kA current pulse train is illustrated in figure 3. The graph shows the last successful surge current pulse train of a device in red, and the failure in black. The device fails during the third pulse, presumably due to thermal overload. The failure is characterized by the loss of reverse blocking capability after that third current pulse.



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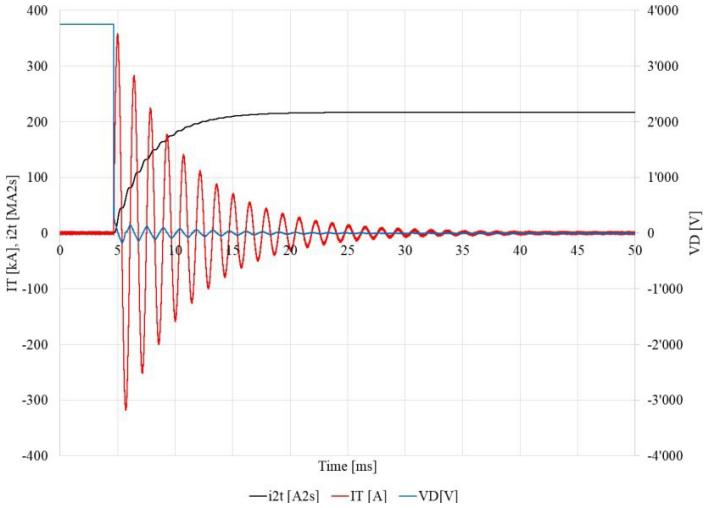
03 23 kA current pulse train



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05 Thyristor current and voltage waveforms from the surge $\hat{i}_{max}$ = 363 kA, i^2t_{max} = 217 MA^2s

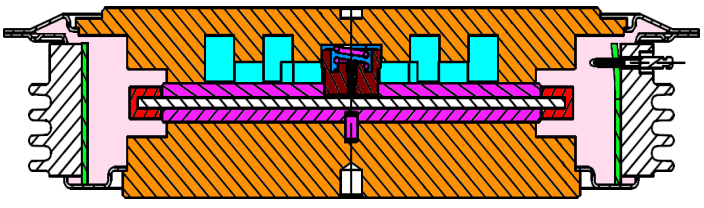
The bypass device is operated at zero duty cycle under a DC-voltage that can reach 4.6 kV. The wafer was designed with an 8.5 kV blocking capability to prevent cosmic ray failures.

Housing design

The study found that the most important factor to achieve triggered non-rupture conformance at the highest energy levels was to make space inside the cathode pole-piece. This space acts as an expansion volume that both decreases the gas pressure and improves heat transfer from the plasma to the cathode pole-piece. Figure 4 shows how the expansion volume (cyan) is created in the lid (upper orange region). Further improvements indicated in figure 4 are:

- The ceramic walls are lined with a (green) silicone rubber strip to protect the wall from cracking due plasma that escapes the pole-piece despite the presence of the expansion volume.
- The cathode sealing flange is protected by a labyrinth seal between the lid and the ceramic wall.

The design shown in figure 4 passed all case non-rupture tests, corresponding to $i^2t \approx 215\ MA^2s$ and $\hat{I}_{max} \approx 360$ kA. This capability exceeds requirements, so it was not extended to provoke actual ruptures of the final design. The waveforms in figure 5 illustrate an example surge at the limit of the capability. Figure 6 shows an image of the lid developed for the project to the right.



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04 Cross-sectional illustration of the assembled final housing

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06 Pole piece with expansion volume to contain plasma blast

Three housing sizes (102-, 120- and 150-mm flange outer diameters) were fitted for the selected wafer size (⌀ ≈ 75 mm). The expansion trenches were only tested with the 120 mm housing.

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07 Case non-rupture capability achieved

Reliability

In operation the device requirements are trivial in comparison to other devices. Thanks to the low active losses, the device operates at approximately the ambient temperature, resulting in trivial load- and temperature cycling requirements. After triggering, its short-circuit failure mode (SCFM) remains low-ohmic until the next planned maintenance. To verify the stability, SCFM testing was performed at maximal foreseen phase current, 1300 A_{RMS}, for over a year. A range of different variants were tested: hermetic and punctured, as well as with and without the wafer sandwiched between 0.5 mm thick aluminum foils. With monotonous on-state voltages varying between 0.1 and 1.75 V, all devices passed the electrical tests, but their appearance after the test varied substantially. The use of aluminum foils had a large impact on the post-SCFM appearance. The use of foils, however, could not be justified in the final design, since they did not measurably improve electrical SCFM performance.

Conclusion

A semiconductor-based bypass device for use in MMC topologies with a cell voltage of up to 4.6 kV DC is proposed. The device will not rupture up to, or exceeding, 363 kA or 217 MA^2s, provided it is triggered during the fault. The key to achieving such high non-rupture ratings is to create a volume inside the pole-piece for the byproducts of the electric arc to expand and cool. After a fault, the device displays a stable short circuit for more than a year, conducting 1300 A_{RMS} with a voltage drop below 1.75 V_{RMS}.

References

[1] “Rugged MMC converter cell for high power applications”, Ødegard, Weiss, Baumann and Wikström, Proc. EPE 2016.
[2] “An 8.5kV Sacrificial Bypass Thyristor with Unprecedented Rupture Resilience”, Proc. ISPSD 2019.
[3] IEC international standard 60747-6, Section 6.3.6, “Peak case non-rupture current”. http://www.iec.ch.

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