High power density SiC power module for Formula E: requirement, design considerations and the test results

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Abstract

Power converters utilized in Formula E, due to the demanding requirements and competitive nature, require fully optimized power semiconductor modules, including the latest device and packaging technologies. In this paper, firstly, the key requirements of Formula E are presented and compared with the standard electric vehicle applications. In the next step, the design considerations such as semiconductor device selection, electromagnetic design, switching conditions and losses, cooling schemes and effect of packaging component selection on the thermal resistance, module integration and power density are discussed. Finally, the characteristics and the capabilities of the RoadPak module optimized for utilization in a Formula E power inverter are demonstrated.

1 Introduction

Formula E is an electric powered race car championship that began in 2014 and is currently known as “ABB FIA Formula E Championship” after ABB sponsorship in 2018 [1]. Due to its competitive nature, the teams and FIA manufactures are always keen on ever better motors and inverters, in which the power module (PM) is a key component. Despite considerable advancement in power modules for the passenger electric vehicle (EV) market in the recent decade, special attention and optimization is required for Formula E race car application due to its specific requirements. As an example, in the fifth race season (2018/2019) of the Formula E, a so-called attack mode was introduced which can be activated during the race if the driver crosses a specified track on the race circuit. It allows additional 35 kW power on the motor for a certain duration to create a possibility for strategic maneuvers and take over. The use of attack mode is monitored (when a driver has activated the attack mode, the Halo device on top of the cockpit is showing a blue illumination) and needs to be compensated during the race by energy management. For optimum use of such strategies, e.g. the 35 kW extra power of attack mode, additional power from the drive train is required which consequently loads the PM furthermore underlining the importance of PM in such a demanding application.

In this paper, firstly, the PM-focused requirements for the Formula E application are briefly compared to those of the standard EV. The design considerations and possible scenarios to upgrade a PM for high power to weight are discussed and quantified. Finally, it is demonstrated how these improvements are applied on the Hitachi ABB Power Grids (HAPG) RoadPak power module to boost further the power density for Formula E application.

2 Requirement specification

The standard automotive is a highly regulated market in which several standards were developed during decades to ensure the end customer requirements are fully met. Due to long service life, mass volume nature as well as high cost of recalls in case of problems, a similar approach has been started for the passenger EV. Nowadays, in addition to original equipment manufacturer (OEM) requirements, several efforts focused to standardize PM requirement for EV application, e.g. the well-accepted ECPE guideline AQG324 for PM qualification [2]. However, due to the competitive nature of formula E, the focus is mainly on the excellent performance of the PM and the overall system during a race season, while the requirements like long-term reliability and cost are less critical compared to an EV application. Herein, a higher attention is devoted to power density or in other words current per unit surface, weight to

power ratio and immediate full power availability in a situation like race start. Nevertheless, Formula E inverters show higher flexibility in the overall design thanks to more relaxed volume production requirements as well as more manual inverter assembly process. In addition, there is typically more freedom in cooling fluid selection and cooling characteristics due to higher minimum inlet coolant temperature, as well as higher allowed pressure drop in the cooling system.

The aforementioned specific requirements indicate the need of a dedicated design consideration and optimization to maximize the performance of PM for this application which will be discussed in the next section.

3 Design considerations

3.1 Chip characteristics effects

Although inverters were typically designed based on Si-IGBT modules for the first race seasons, the SiC MOSFET technology has been considered as a promising alternative technology. In fact, the low losses of SiC MOSFET switches compared to the current Si-IGBT has made them very attractive alternatives, especially for applications where low weight and enhanced efficiency are critical, such as Formula E. For this reason, the Hitachi ABB Power Grids RoadPak 1.2kV SiC MOSFET half-bridge module (shown in Fig. 1) was considered here as the baseline design for further specific optimization. Note that the baseline RoadPak module contains the latest generation SiC MOSFET with low losses and high reliability to serve the eMobility market [3].

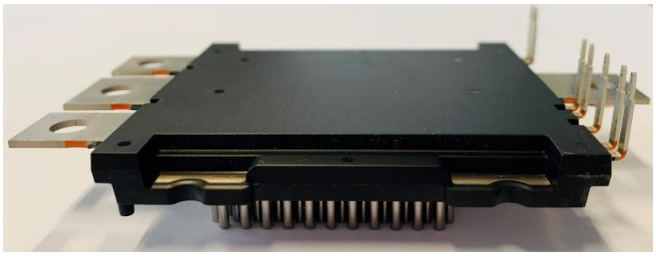

Fig. 1: The HAPG RoadPak 1.2kV SiC MOSFET half bridge module (size<70mmx75mm)

In order to increase the maximum current rating (I_{rms}) or power density, the first option is indeed increasing the effective chip surface. Although, the RoadPak baseline design for EV market is based on 8 parallel SiC chips, it allows scaling up by increasing the number of parallel chips to 10 without changing the outline. Note that increasing active surface of individual SiC chip is less practical, since the size of SiC MOSFETs is typically limited due to yield challenges in their manufacturing (typically active area of SiC MOSFET currently in market is <30 mm^2).

Figure 2 shows the effect of number of parallel chips on current rating for specific operating conditions. In all cases of Fig. 2, the maximum current rating is defined by the maximum allowed junction temperature of the considered SiC MOSFET i.e. 175 °C.

Comparison of thermal simulation results in Fig. 3 indicates that adding parallel devices leads to a decrease in heat spreading and accordingly increase in thermal resistance (R_{th}), because of so-called thermal crosstalk between neighboring chips. Therefore, 10 chips per side was considered here, since further increase in number of parallel chips in such a module with high chip population leads to less gain in current rating.

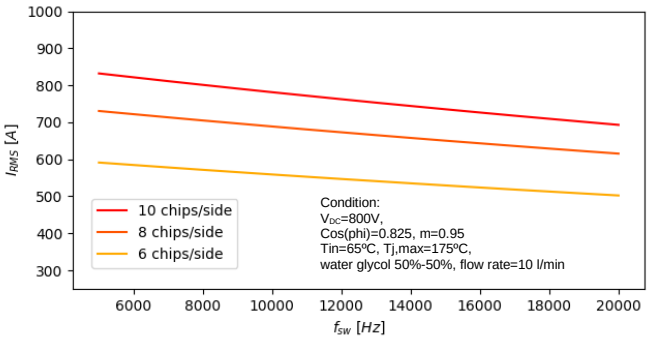

Fig. 2: Relative current rating based on number of chips in parallel versus switching frequency in a HAPG RoadPak 1.2kV module design.

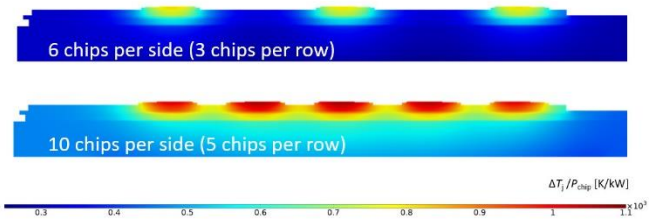

Fig. 3: Comparison of R_{th} per chip ($\Delta T_j/P_{chip}$) in case of RoadPak with 6 or 10 parallel chips showing effect of thermal crosstalk on the thermal performance.

Due to the thermal limit, a proper understanding of the losses is the key for device selection as well for design optimization. In this regard, Fig. 4 presents the contribution of conduction losses (P_{cond}),

switching losses (P_{sw}) and lead losses (P_{lead}) at two defined switching frequencies i.e. 10 kHz and 20kHz for RoadPak PM variants with 10, 8 and 6 chip per side. Analysis of Fig. 4 shed light on the key factors for enhancing power density, which is shortly explained here.

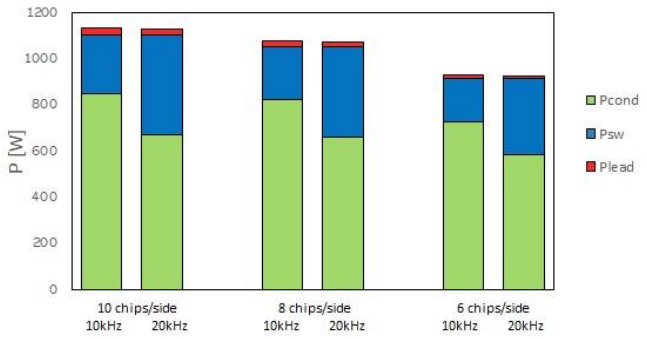

Fig. 4: Allotment of different losses (conduction, switching and lead) in the PM at rated current.

In the condition considered here, the conduction losses play the most important role in limiting the maximum current capability, which is mainly function of the channel on-state resistance of the MOSFETs ($R_{DS,on}$) during conduction according to $P_{cond}=R_{DS,on}.I_{rms}^2$. In this regard, selection of SiC MOSFET with the lowest possible $R_{DS,on}$ is crucial. Note that the $R_{DS,on}$ at the maximum allowed junction temperature of the device ($T_{j,max}$) is decisive when maximum current rating is the focus. However, the known tradeoff between $R_{DS,on}$ from one side and cosmic ray FIT rate, short circuit capability and gate oxide reliability from the other side must be carefully considered [4].

For a better understanding, the current rating of the power module with different $R_{DS,ON}$ at different cooling conditions are compared in Fig. 5. The data here show that a 20% decrease in the SiC MOSFET $R_{DS,on}$ can lead to ~10% increase in the maximum current rating of the PM in a typical operating condition.

At the second position, switching losses are considerable, as shown in Fig. 4. The considerably lower switching losses, including turn-on (E_{on}) turn-off (E_{off}) and reverse recovery losses (E_{rec}) is one of the main reasons which make the SiC-based PMs attractive compared to Si IGBTs. Obviously the higher the switching frequency is, the higher the total switching losses in power module will also be. However, for the selection of optimal switching frequency, a system view considering the noises and motor losses should be considered.

3.2 Effect of cooling characteristics

As previously demonstrated, the maximum current capability is mainly limited by reaching the $T_{j,max}$. Herein, selecting chips with higher $T_{j,max}$ and thermal management i.e. decreasing thermal resistance of module (R_{th}), are therefore one of the main improvement aspects.

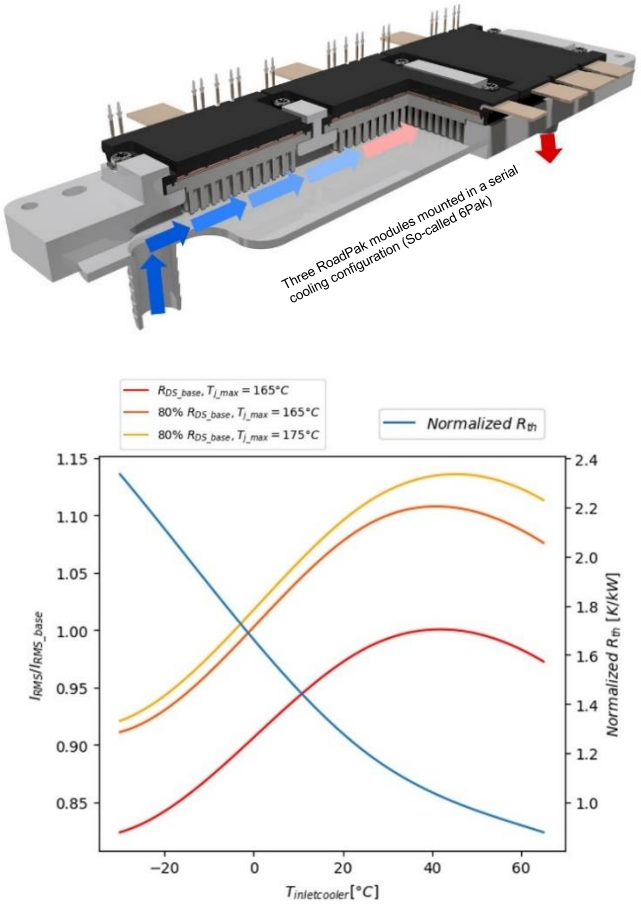

Fig. 5: Effect of $R_{DS,on}$, chip max allowed junction temperature ($T_{j,max}$) and coolant inlet temperature on module current rating.

Most of the SiC MOSFETs in the market are rated at $T_{j,max}$ of 150-175 ºC. For better understanding of the $T_{j,max}$ effect, the data in Fig. 5 show that 10°C higher $T_{j,max}$ allowance (from 165°C to 175°C) can lead to ~2-5% increase in I_{rms} at different R_{th} and operating conditions. The current RoadPak module is rated at 175 ºC, although the trend is to increase the $T_{j,max}$ toward 200 ºC.

Regarding the R_{th} decrease, main considerations are PM packaging, the cooling system and conditions which are discussed below.

Coolant inlet temperature (T_{in})

Although lower coolant inlet temperature provides higher margin toward $T_{j,max}$ i.e. higher $T_{j,max}$-T_{in}, it is not necessarily helpful as the viscosity of typical coolants in the EV inverters is higher at low temperature which causes an increase in R_{th} and consequently decrease in I_{rms}. The data in Fig. 5 show the effect of T_{in} on the R_{th} and rating. As an example, the R_{th} and I_{rms} are respectively ~200% higher and ~25% less at -20 ºC when compared to 40 ºC.

Type of the coolant fluid

Contrary to standard EV applications, operation in very low environment temperatures (e.g. -30°C) is less relevant for Formula E. Therefore, a careful selection of the coolant, e.g. by using less amount of glycol in a water-glycol mixture can be very beneficial due to its lower viscosity and better cooling performance. In addition, the coolant with lower viscosity decreases the pressure drop in the system which can lead to need of smaller and lighter pump. The data in Fig. 6 show the effect of glycol content on the R_{th} and pressure drop in a 6Pak configuration of Fig.5. The benefit of low glycol- content coolant is more profound at lower T_{in} due to less viscosity increase.

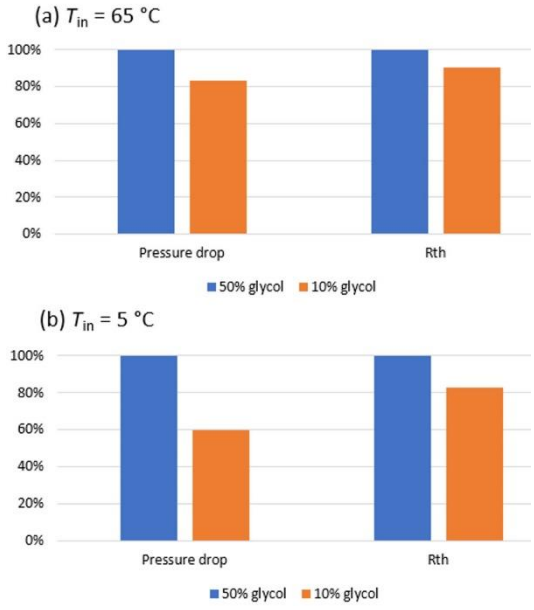

Fig. 6: Effect of coolant type namely glycol content on the module cooling performance at 2 different inlet temperatures.

Flow rate and pressure drop

The effect of flow rate on R_{th} and pressure drop for a typical EV system is shown in Fig. 7. Obviously, a higher flow rate will lead to better cooling, therefore lower R_{th}, but simultaneously increase the pressure drop across the cooler. With a careful design of the cooling channel (see more information in [5]) as well as using low viscosity coolant, an optimum use of flow rate is achievable in the RoadPak design.

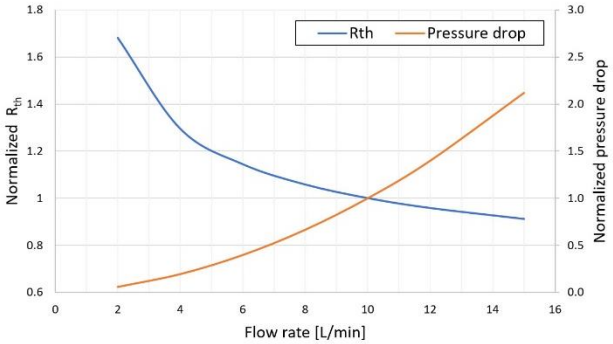

Fig. 7: Effect of flow rate on module cooling performance.

3.3 Packaging components

In order to benefit from the high performance of new SiC MOSFET devices, a package with superior thermal management is required to effectively remove the heat from the chip. Several studies addressed the advantages of direct cooling (either single-side or double-side cooling) for power modules, when compared to the indirect classical approach e.g. with thermal paste [6, 7]. A serial one-side cooling with optimized pin fin approach due its high cooling performance and easy integration in the invertor was considered here in RoadPak design. The cooler design and cooling scheme are presented in [5]. Beside the cooling scheme, various design decisions like die-attach materials and thickness, substrate ceramic type and base plate design have profound impact on the R_{th} of PM.

In addition to its considerably higher reliability during power cycling, the sinter die attach material provides lower electrical resistance and higher thermal conductivity when compared with the classical soldering approach [8] and therefore selected for the RoadPak. Considering a thin and dense silver sintered layer for die attach (resulting in thermal conductivity of 320 W/mK), a reduction of ~5% in R_{th} is achieved in comparison with the soldering.

Copper and AlSiC are among the most common materials used as heat sink / base plate of PMs. As shown in Fig. 8(a), using an AlSiC base plate decreases the thermal performance by ~35%, although it is ~70% lighter, when compared with a copper base plate with analogous pin fin design. Due to considerably higher thermal performance of the copper base plate caused by its higher thermal

conductivity (385 W/mK for Cu versus 180 W/mK for AlSiC) and better heat spread effect, it was selected for the RoadPak design. Note that, the modules with copper base plate are typically expected to have lower lifetime in passive power cycling due to its high coefficient of thermal expansion (CTE), or namely higher CTE mismatch with adjacent ceramic substrate [9]. However, by careful selection of encapsulation material in the RoadPak, namely by selecting mold compound which matches the effective CTE of the overall power module design, the negative impact of high CTE of Cu base plate was effectively compensated.

The alumina DBC substrates are the most common ceramic materials for substrate of PMs. However, active metal brazed (AMB) substrates with aluminum nitride (AlN) ceramic and or silicon nitride (Si_3N_4) ceramic are shown to be significantly more reliable than alumina DBC substrates, especially over large temperature swings, e.g. in thermal shock [10]. The data in Fig. 8(b) compares the thermal performance i.e. R_{th} of the RoadPak module, considering the aforementioned ceramic material options indicating ~20% lower R_{th} in case of using AlN or Si_3N_4 instead of Al_2O_3 with the same thickness.

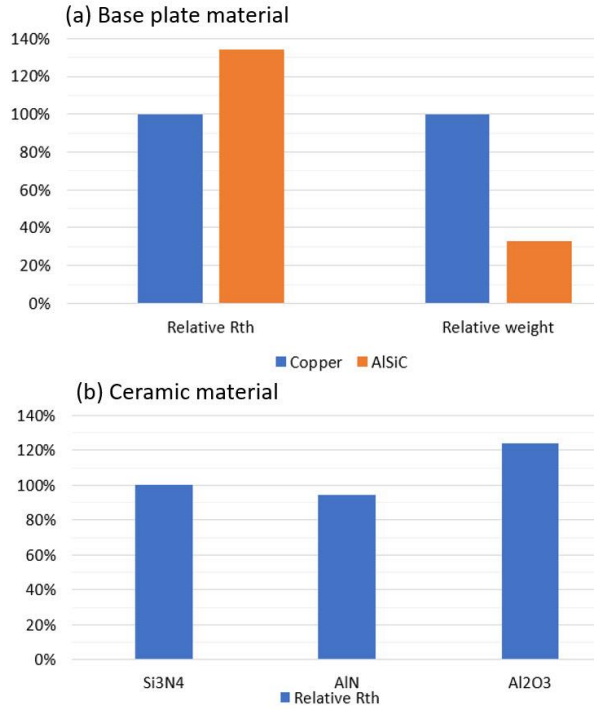

Fig. 8: Effect of (a) base plate, (b) ceramic insulation materials selection on thermal resistance and weight of power module [condition: T_{in}=65°C, Flow rate=10 L/min, water 50% glycol 50%]

The latter is due to the difference in the thermal conductivity of the selected materials (18 W/mK for Al_2O_3, 105 W/mK for AlN and 60 W/mK for Si_3N_4 at 125 ºC). Considering the high reliability and the superior toughness of Si_3N_4 which makes it suitable for die attach sintering process, it was selected for RoadPak design. Note that despite higher cost of Si_3N_4 per se, it consequently leads to lower cost per current of the PM.

3.4 Electromagnetic design consideration

Looking back at Fig. 4, the switching losses of the PM are the second important factor from performance point of view. Herein, in addition to the switching frequency, the switching energy (E_{on}, E_{off}, E_{rec}) is a key parameter. Beside the device characteristics, the latter highly depends on the maximum allowed switching speed or in other words, the dV/dt during the turn-off/on event. Note that, as much attractive the use of high power SiC MOSFET is, their utilization in high power modules requires particular care when designing the layout in terms of electromagnetic (EM) design. Specifically, due to small size of a SiC MOSFET (typically <30mm^2), several single chips must be paralleled to reach high current rating. Upon paralleling a high number of devices, however, the problem of inhomogeneous switching arises in high speed conditions, leading to increased oscillations and parasitic effects, such as the parasitic turn on of a device. Such undesired effects may finally lead to current derating or limiting of the switching speed, thus reducing the low loss advantages of SiC MOSFETs [3]. For this reason, in addition to reducing the source self-inductance, the effect of the mutual inductance of all the current paths with the gate path of each chip was considered and optimized in the RoadPak design.

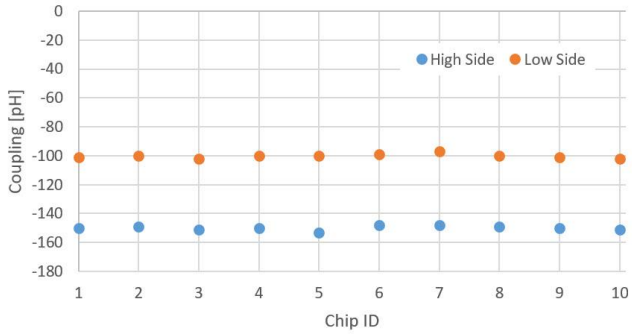

Fig. 9: Coupling between gate-source and drain-source path per chip for the high-side and low-side of RoadPak module with 10 parallel chip per side

The result of the optimization is summarized in Fig. 9 indicating that the total gate-source coupling is well balanced between chips for the low side and the high side within a window of <10 pH. The negative value of the total coupling inductance of Fig. 9 was selected to achieve a small negative feedback on the gate. This will lead to apply a negative voltage on the gate. While a very high negative value would cause the module to become too slow and the overall switching losses too high, the slight designed negative feedback will decrease the gate voltage, effectively slowing down the turn on of each individual chip in a controlled manner. The same analysis can be done for a MOSFET turn off event. The negative gate coupling prevents the current of each individual chip to turn off too fast, therefore increasing balancing of the current and reducing the oscillations.

As an example, the data in Fig. 10 show the measured E_{off} in RoadPak double pulse test at different switching speeds and currents. The EM optimized design enables controlling the switching speed by adjusting the external resistance at the Gate Driver Unit (GDU), which gives flexibility to match the customer requirements and also enables switching up to high dV/dt of ~35 V/ns in order to minimize switching losses without critical oscillations.

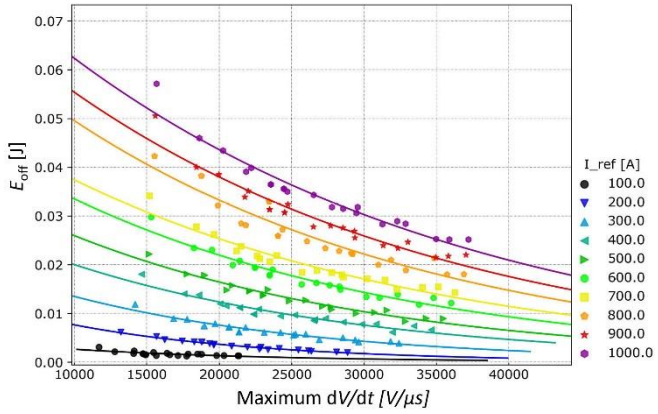

Fig. 10: Measured E_{off} in RoadPak at different switching speeds and currents from double pulse tests

4 Result summary

The RoadPak 1.2kV design for Formula E was optimized and the module was manufactured using learnings of previous chapters, aiming to reach maximum possible power density. The data in Fig. 11 show the validated Z_{th} curve for the optimized 6Pak design, considering the hottest chip of module and also the average T_j of the chip on the same side in a 6Pak configuration. Thanks to the improvements on the PM thermal management and overall cooling system, an $R_{th,max}$ of <83 K/kW was achieved for the conditions shown in Fig. 11. The minor difference between average Z_{th} and the hottest chip Z_{th} indicates the homogenous cooling of the parallel devices. The aforementioned low R_{th} allows an operating point of I_{rms}>900A at the operating conditions (V_{DC}=800V, f_{sw}=10 kHz, T_{in}=45ºC, CosΦ=0.825, m=0.95).

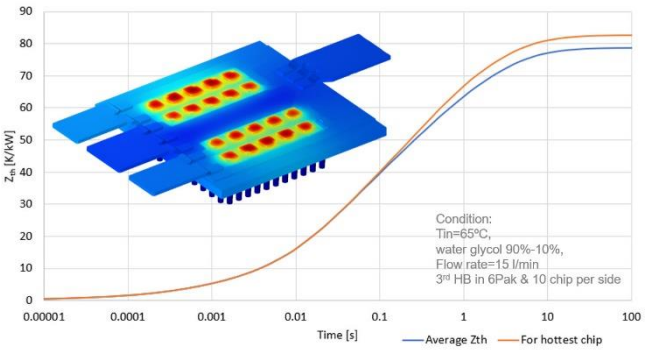

Fig. 11: Validated Z_{th} curves for RoadPak module.

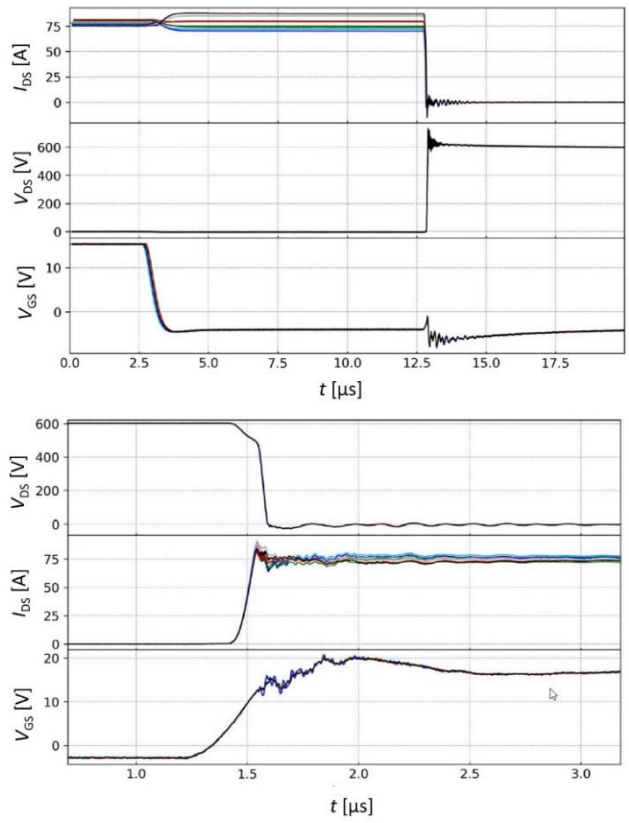

Fig. 12: Measured current in each individual chip in a RoadPak 1.2kV HB design with 10 parallel SiC MOSFE during (a) low-side MOSFET turn on, (b) high-side diode turn off.

In order to validate the EM-optimized layout, the internal current distribution of the 1.2kV RoadPak module was examined using an open power module i.e. without mold compound. For this purpose, the Rogowski coils were used to measure the current for each chip individually. Voltage was measured at auxiliary terminals. The conditions for the test are 600V, 600A, 25°C. Measurement at a higher voltage was not possible due to the absence of mold compound in the open modules. As examples, Fig. 12 shows the measured current in each chip in a RoadPak with 10 parallel SiC MOSFET during low-side MOSFET turn on and high-side diode turn off.

In the Fig. 12 (b), the distribution of current is initially according to $R_{DS,on}$ until 3.5µs. Then the channel is turned off and the distribution of the current is according to body diode on-state until the diode turn-off event is initiated at 13.5µs. The result in Fig. 12 confirms a harmonized switching event for all the parallel chips and excellent static current sharing thanks to the well EM optimized layout design which allows fast switching of the module (as shown in Fig. 10) and leads to high reliability of the power module.

5 Conclusion

Optimization of power semiconductor module in order to maximize the current rating, as well as power density per unit weight and reliability for a demanding application like Formula E, requires a multidisciplinary approach considering different aspects, comprising device selection, electromagnetic optimization, careful selection of packaging materials, coolant fluid as well as cooling scheme. In the current paper, the effect of various features on the overall power module performance were discussed and it was demonstrated how the half-bridge 1.2kV RoadPak module with a foot-print smaller than 70mmx75mm can effectively deliver I_{rms} of more than 900A at the operating point with clean switching, which makes it a benchmark SiC power module.

6 References:

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