Rugged LV Trench IGBT with Extreme Stability in Continuous SOA Operation: Next Generation LV Technology at Hitachi ABB Power Grids

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Abstract

A new generation low voltage (LV, 1200 V, 150 A rated) fine pattern (FP, active trench distance < 2 µm) trench gate insulated gate bipolar transistor (IGBT) has been developed and optimized at Hitachi ABB Power Grids for improved on-state and turn-off losses, robustness and long-term performance reliability. In this work, different IGBT protection cell designs have been systematically investigated. A new design concept is proposed and experimentally investigated with the purpose of realizing a robust degradation-free design without comprising the device performance. Our new state-of-the-art FP LV trench IGBT has been investigated under repetitive harsh switching conditions. The new design has been found to have a stable performance over time and be minimally affected by dynamic avalanche degradation even when switched with a 4 x I_{nom} current.

1 Introduction

Development of silicon based high power devices is driven by customer need to guarantee a high safe operating area (SOA), high temperature operation for increased output power and long lifetime. The long-term performance stability and drift of trench devices is particularly important [1]. Hot charge carrier injection into the gate oxide is the typical trench degradation mechanism associated with the loss of long-term stability in trench IGBTs [2, 3]. Injected charged carriers can become trapped at the silicon-oxide interface specially at the trench bottom. During turn-off, the current consists mostly of holes being displaced during the expansion of the depletion layer. Holes are accelerated towards the trench bottom by the high electric field in the depletion layer especially during the over-voltage phase of hard turn-off switching events [2]. For devices with low turn-off losses (high on-state losses) the strength of hole displacement can become large due to the high electric field gradients that can be formed in the depletion layer resulting in high *dV/dts*. For devices with low on-state losses and strong dynamic avalanche the expansion of the depletion zone is slowed down by the high generation of new electron-hole pairs that also enhances gate oxide degradation [4]. It has been proposed before that placing a p-doped region (p-well) on the outer side of the active (bottom) trenches serves to ensure the long-term stability and reliability of trench IGBT devices by protecting them against dynamic avalanche degradation [1, 2]. This is one of the key components of the different IGBT protection cell designs that have been systematically investigated here via TCAD simulations. Furthermore, a new design concept ("plasma flow control") is proposed and experimentally investigated. For this purpose, devices in different places in the technology trade-off curve and hence different dynamic avalanche characteristics have been investigated under repetitive harsh switching conditions. Even though these are not standard conditions typically experienced in the field, the purpose of these harsh repetitive switching tests is to accelerate the degradation so we can extrapolate lifetime stability at less extreme conditions in the field.

2 The new 1.2kV FP Trench IGBT

As previously stated, different approaches have been researched to protect trench IGBT devices against dynamic avalanche such as: placing a p-doped region on the side opposite of the channel of the active trench (gate-biased) [2], using a thicker gate oxide near their bottom [3] or using adjacent dummy (emitter-biased) trenches for electrostatic shielding [5]. In here, to minimize the impact of dynamic avalanche we seek to reduce

the electric field or divert injected holes away from the active trench during the turn-off transient by:

- introducing a combination of additional dummy trenches and optimized doping concentrations near the active trenches for electrostatic shielding of the active trench.
- introducing a novel 'plasma flow control' feature to reduce hole density near the active trench.

2.1 Simulation Study

The role of the dummy trenches and p-well in protecting the device against dynamic avalanche was investigated using TCAD device simulations (Synopsys Sentaurus TCAD 2018). Three different trench IGBT designs (*Designs 1 - 3*, Fig. 1) were considered.

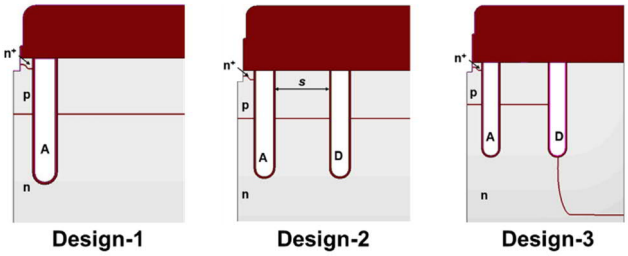

Fig. 1: Schematic diagram of different IGBT protection cell designs investigated using TCAD simulations.

Design-1 consists of only an active (denoted by '*A*') trench (unprotected design), *Design-2* features a dummy trench (denoted by '*D*') placed at a distance *s* from the active. *Design-3* consist of additional deep p-well below the dummy trench. In addition, the new 'plasma flow control' feature is applied to *Design-2* and *Design-3* for the purposes of investigating how dynamic avalanche is affected during turn-off. All other design paraments were kept constant.

For this study, avalanche generation near the active trench during the switching event was explored as a measure of device degradation. As can be seen in Fig. 2., in comparison to the 'unprotected' *Design 1*, the avalanche generation near the active trench is reduced by more than 2 orders of magnitude for the proposed 'protected' *Design 3*. *Design-3* with both dummy trench and p-well is better protected against degradation as compared to the other designs.

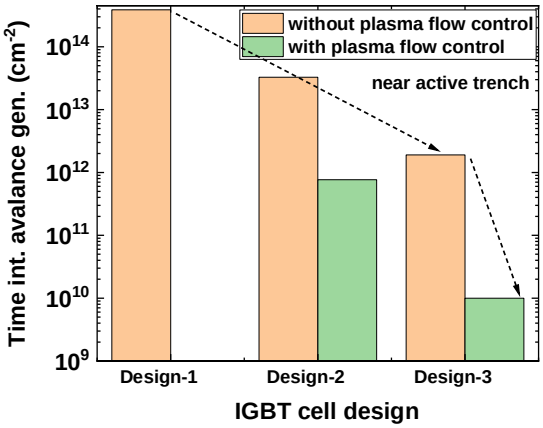

Fig. 2: Plot showing the total time integrated avalanche generation near the active trench during the turn-off switching event for different designs.

Our novel 'plasma flow control' design plays an important role in reducing avalanche generation by another two orders of magnitude as can be seen in Fig. 2. This is accomplished by diverting a significant number of holes away from the active trench during the turn-off transient. In this situation, the dummy trench shares a significant part of the avalanche generation as shown in Fig 3.

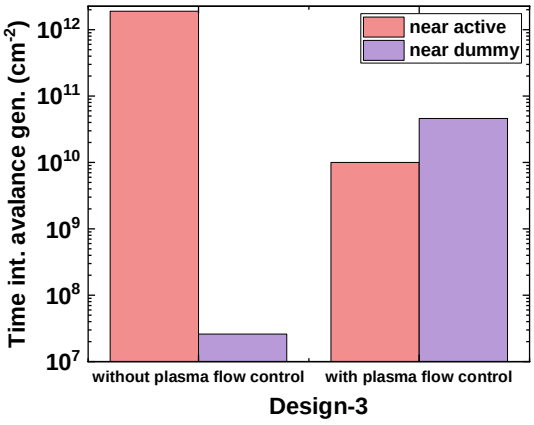

Fig. 3: Plot showing the avalanche generation at the active and dummy trenches for *Design-3* with and without plasma flow control.

Avalanche generation near the active trench was found to increase with increasing distance between the dummy and active trenches (Fig. 4). Therefore, it is desired to place the dummy trench as close as possible to the active trench to protect the latter from the impact of dynamic avalanche for better long-term stability and ruggedness.

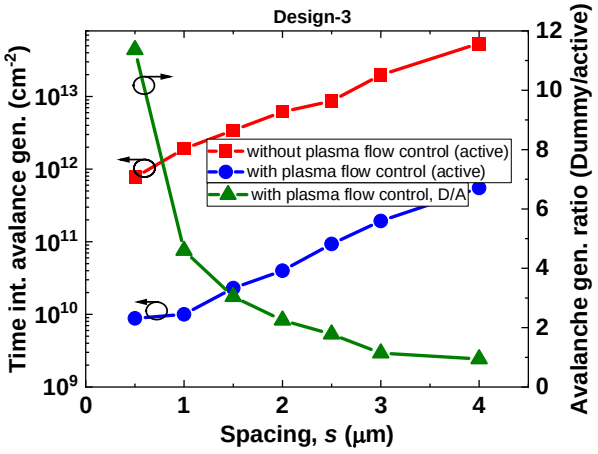

Fig. 4: Plot showing the avalanche generation near the active trench with varying spacing between the dummy and active trenches for *Design-3*.

Devices with the 'plasma flow control' feature, consistently show lower avalanche generation (Fig. 4 for *Design-3*) for all varied trench spacings. Furthermore, an increasingly less percentage of the avalanche generation is shared by the dummy trench when it is moved further away from the active trench.

The proposed *Design-3* has furthermore an added advantage of reduced Miller capacitance [5] thereby resulting in lower switching losses. It therefore also lies on a more favorable place in the technology curve as shown in Fig. 5 (same $V_{ce\text{-}sat}$ but lower E_{off}) as compared to the unprotected *Design*-1.

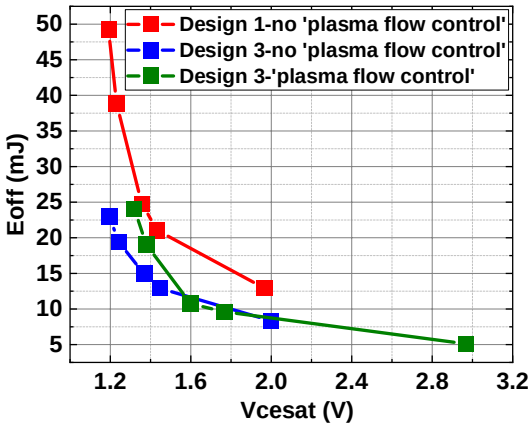

Fig. 5: Simulated technology curve (125 °C) for *Design-1* and *Design-3* (with and without 'plasma flow control').

2.2 Device Performance

Design-3 ("protected design") was also experimentally realized to verify the simulation findings. The p-well protecting the active trench pair from degradation during repetitive switching events in *Design-3*, in this design is placed right next to the dummy trench. Like this, lateral dopant diffusion during processing annealing steps can be further stopped first by the dummy outer trenches guaranteeing that the p-well implant never merges with the p-channel of the active trench. Such design, when optimized and together with an excellent gate oxide quality, leads to a device with high blocking capability (> 1400 V) and stable switching performance over time. It is minimally affected by the amount of dynamic avalanche during hard switching applications as will be shown later. It can be furthermore be manufactured with wide processing margins.

Design-3 devices in different places in the technology trade-off curve (*A, B, C*, Fig. 6. measured at T_j = 150 °C, 8.2 ohm, 150 nH), and hence different dynamic avalanche characteristics have been investigated. Different places in the technology curve could be achieved by simple changes in process parameters, such as anode doping or trench depth.

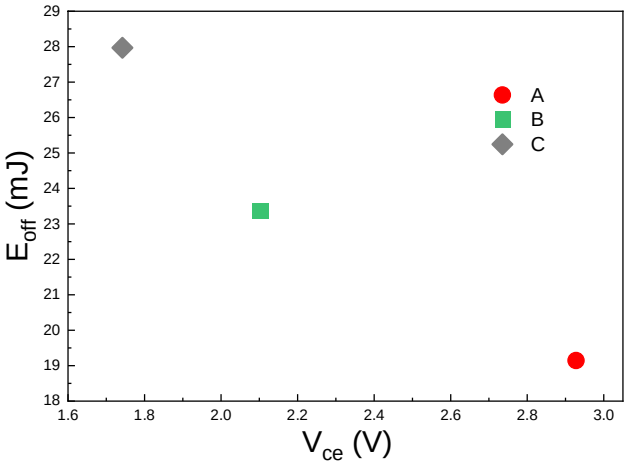

Fig. 6: Technology trade-off curve measured at V_{cc} = 600 V, I_c = 150 A and T_j = 150°C, 8.2 ohm, 150 nH. Devices *A, B, C* are experimentally realized variants of proposed *Design-3*.

Figure 7. Shows the turn-off waveforms measured under reverse biased safe operating area (RBSOA) conditions (300 A, 900 V, 8.2 ohm, 150 nH, 150 °C) for different devices *A, B and C*.

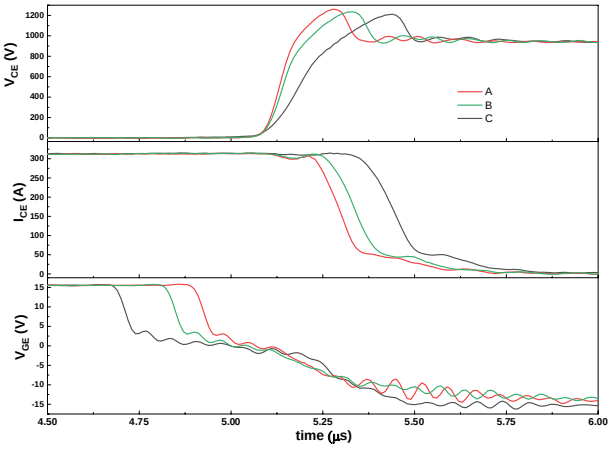

Fig. 7: RBSOA turn-off waveforms measured at V_{cc} = 900 V, I_c = 300 A and T_j = 150 °C, 8.2 ohm, 150 nH.

Strong avalanche can be observed in all tested devices but specially on device C. Dynamic avalanche happens when IGBTs are switched at high currents with high *dV/dts* and can be identified from the voltage turn-off switching waveform. The curvature in the voltage turn-off waveform (reduced *dV/dt*) during voltage buildup points out to dynamic avalanche where the plasma sweep-out rate is slowed down by the generation of new electron-hole pairs, slowing down the turn-off process [6].

3 Repetitive Switching Performance

The behavior and long-term stability performance of the same devices was investigated under dynamic repetitive stress conditions. Switching was performed at 150 °C, which is the nominal junction temperature. The device in the field will be operated at high temperatures (≥ 125 °C) for a great majority of its lifetime. It is important to investigate device degradation under stress conditions to be able to predict the lifetime of the device and to be able to ensure its long-term stability. For industrial applications with a lifetime of 15 years it's estimated that devices would be exposed to approximately 1 million switching events with twice the rated current [3]. In here devices were first switched 100 k times at 125 % V_{nom} = 750 V and 150 % I_{nom} = 225 A conditions (150 A nominal rated current). Electrical parameters were extracted in an interval of 1000 stress pulses.

Figure 8 shows the No significant change in the static and switching behavior was found after 100 k switching pulses for the different devices regardless of their dynamic avalanche characteristics.

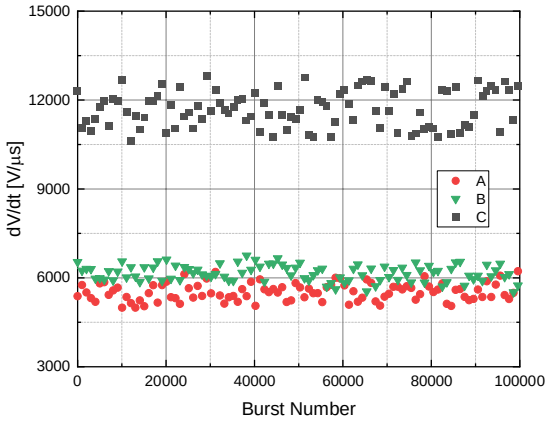

Fig. 8: Evolution of *dV/dt* measured under nominal conditions. The devices are switched 100 k times at 1.25 x V_{nom} and 1.5 x I_{nom}.

Since no degradation was observed after 100k pulses at 1.5 x I_{nom}, the test was repeated at 4 x I_{nom} (600 A) for devices B and C. The higher current level should drastically increase avalanche generation, therefore speeding up degradation.

Figure 9 and 10 show the turn-off and turn-on waveforms before and after 50 k and 100 k switching pulses measured under nominal conditions (150 A, 600 V) for device B and Figure 10 and 11 respectively for device C.

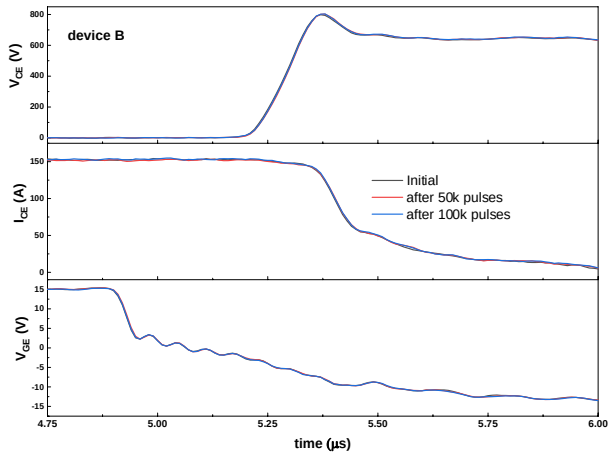

Fig. 9: Turn-off waveforms for device B measured at V_{cc} = 600 V, I_c = 150 A and T_j = 150 °C, 8.2 ohm, 120 nH before and after 50 k and 100 k pulses. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

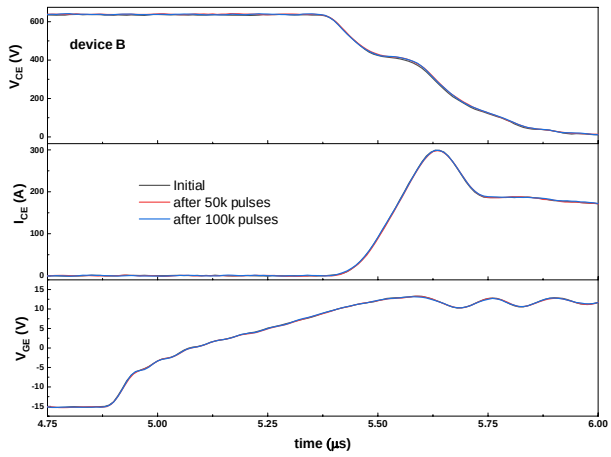

Fig. 10: Turn-on waveforms for device B measured at V_{cc} = 600 V, I_c = 150 A and T_j = 150 °C, 8.2 ohm, 120 nH before and after 50 k and 100 k pulses. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

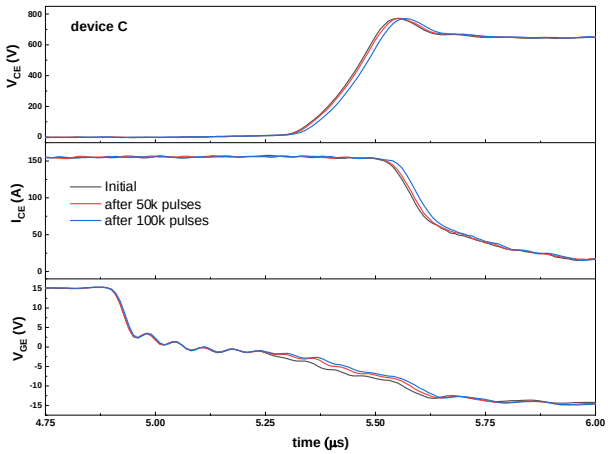

Fig. 11: Turn-off waveforms for device C measured at V_{cc} = 600 V, I_c = 150 A and T_j = 150 °C, 8.2 ohm, 120 nH before and after 50 k and 100 k pulses. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

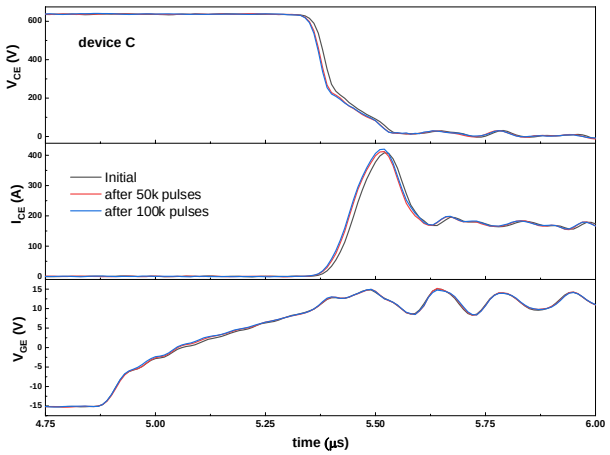

Fig. 12: Turn-on waveforms for device C measured at V_{cc} = 600 V, I_c = 150 A and T_j = 150 °C, 8.2 ohm, 120 nH before and after 50 k and 100 k pulses. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

The turn-on and off delay time t_d for device C with stronger dynamic avalanche characteristics changes only slightly over time as. An increase in delay time does indicate nonetheless that positively charged interface traps form at the Si/Oxide interface [1]. The positively charged traps increase the td and slow down the devices.

Charge trapping and oxide degradation can also be manifested in changes in the turn-on *dI/dt* and turn-off *dV/dt*. The carrier density concentration near the trench bottom varies depending on the plasma concentration. Devices with strong dynamic avalanche are expected to degrade the most over time at this point. Two characteristics serve to stop device degradation under certain conditions: the superior quality of the gate oxide that does not allow for a high number of energetic carriers to be injected and trapped and the device design. The use of dummy trenches on the sides of the active trench pair serve to stop the extension of the p-well and merge with the channel. Even though avalanche generation increases hole injection significantly, the active trench seems to be protected enough as to not cause significant damage over time. Figure 13, 14 and 15 shows the *dI/dt*, $I_{c,max}$ and E_{on} evolution respectively measured under nominal conditions (devices are switched 100k times at 1.25 x V_{nom} and 4 x I_{nom}).The strongest deviation of less than 5 % and 10 % was in fact found for device C on the E_{on} and $I_{c,max}$ respectively.

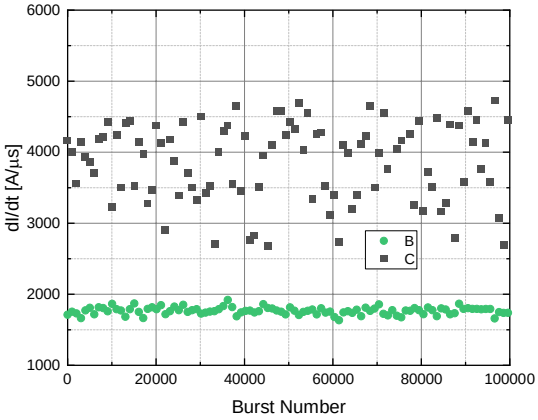

Fig. 13: dI/dt evolution measured under nominal conditions for devices B and C. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

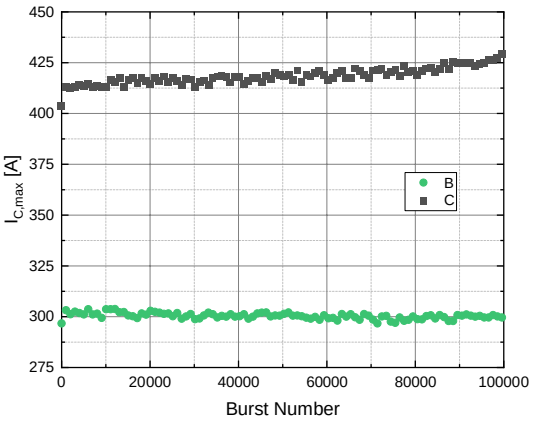

Fig. 14: $I_{c,max}$ evolution measured under nominal conditions for devices B and C. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

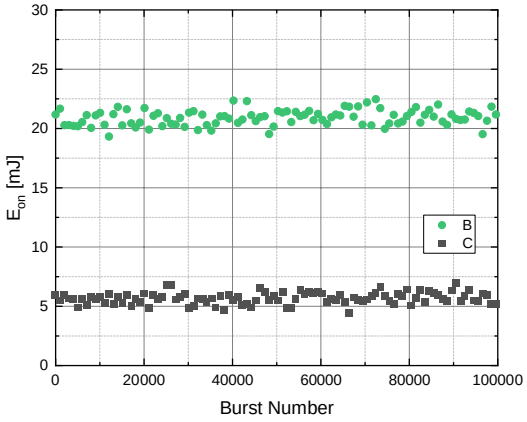

Fig. 15: E_{on} evolution measured under nominal conditions for devices B and C. The devices are switched 100 k times at 1.25 x V_{nom} and 4 x I_{nom}.

4 Conclusion

In here we have presented the next generation FP trench IGBT from Hitachi ABB Power Grids. The new and optimized design is capable of long term and rugged performance regardless of whether the device has strong dynamic avalanche when switched under hard conditions at 1.5 x I_{nom}. It furthermore minimally degrades at 4 x I_{nom} conditions when strong dynamic avalanche is present. The combination of above elements (dummy trench, p-well, 'plasma flow control') in *Design-3* provides a robust design against repetitive RBSOA turn-off pulses and switching losses.

5 References:

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