Comprehensive Analysis of the Impact of Serial and Parallel Cooling on the Thermal Performance of Power Semiconductor Modules

Lluís Santolaria[1], Milad Maleki[1], Athanasios Mesemanolis[1], Antoni Ruiz[1], Edoardo Ceccarelli[1]
[1] Hitachi ABB Power Grids, Switzerland

Corresponding author: Lluís Santolaria, lluis.santolaria@hitachi-powergrids.com

Abstract

A comparison between serial and parallel cooling strategies for consecutive power semiconductor modules was demonstrated by means of Computational Fluid Dynamics (CFD). In the analysis, two different cooling structures were taken into consideration, namely pin fin distribution and meandering channels. All case studies were performed in the scope of the RoadPak eMobility module. The analysis showed that, generally, serial configurations with optimized designs can offer reasonably better thermal performance than equivalent parallel configurations due to the improved usage of the available flow rate. Lastly, the impact of temperature differences between chips on the current sharing is analyzed by means of electro-thermal simulations and infrared thermography measurements.

1 Introduction

Power semiconductor modules are critical components of inverters which generate heat during operation in the form of Joule heating. This heat needs to be dissipated from the modules to avoid excessive temperature in the chip junction and critical packaging components, which could lead to current derating and/or lifetime reduction. Typically, the better the thermal performance of a module is, the higher the current rating can be. Moreover, the thermal performance can significantly affect the reliability of the module, because it has a direct impact on the thermal swing during operation. Therefore, optimizing the design to increase the thermal performance is a key activity during the development phase of any power module. The latter is even more crucial in the case of Silicon Carbide (SiC) power modules like RoadPak [1], due to the high-power density of the package.

The advantages of direct cooling versus indirect cooling (e.g. by using Thermal Interface Material (TIM)) are well discussed and documented [2–3]. Nowadays, there are different direct cooling solutions in the market. Some examples are pin fin serial or parallel cooling, single or double-side cooling or other configurations, such as meander channels or microchannels.

It is well-known that parallel cooling (Fig. 1a) of modules in power inverters – typically 3 modules in a 3-phase inverter – causes loser pressure drop when compared with serial cooling (Fig. 1b), assuming equal boundary conditions (e.g. inlet coolant temperature and flow rate, design parameters, etc.). This is mainly because the total flow rate is divided by the number of modules in the inverter, being the velocity within the cooling structures reduced. The system pressure drop (Δp) is, approximately, function of the square of the velocity within the structures ($\Delta p \sim v_f^2$); hence, reducing the flow velocity will cause a larger relative reduction in pressure drop.

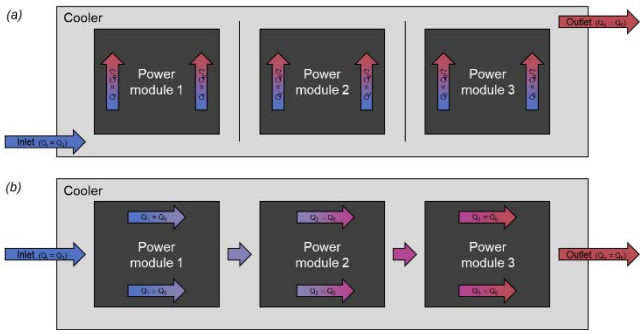

Fig. 1: Schematics of parallel (a) and serial (b) cooling configurations of power modules mounted on a cooler (flow rate Q is indicated for each case).

2 Design of experiment

In this paper, a comprehensive analysis of the thermal performance of a RoadPak module is presented, considering different possible cooling scenarios within a common framework, namely using the Hitachi ABB Power Grids (HAPG)

ISBN 978-3-8007-5515-8

RoadPak module design, stack of layers and material properties.

- **Scenario 1: Serial configuration using pin fin structure**

In this scenario, the power modules were cooled down one after the other in a serial disposition and, therefore, using the whole available flow rate. The module used for this configuration included the current base plate of RoadPak (Fig. 2), an evolution of the previously optimized pin fin structure [4].

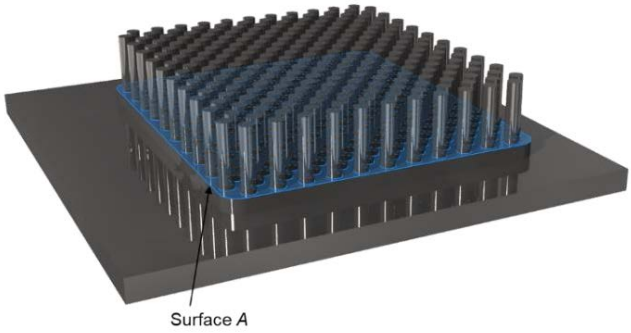

Fig. 2: Base plate with pin fin structures protruding from *surface A* used in RoadPak modules.

- **Scenario 2: Parallel configuration using pin fin structure**

In this scenario, the modules were cooled in parallel and, thus, the coolant flow was distributed among the modules. For all cases, the coolant flow rate below each of the three modules was assumed to be the same, which corresponds to an ideal case.

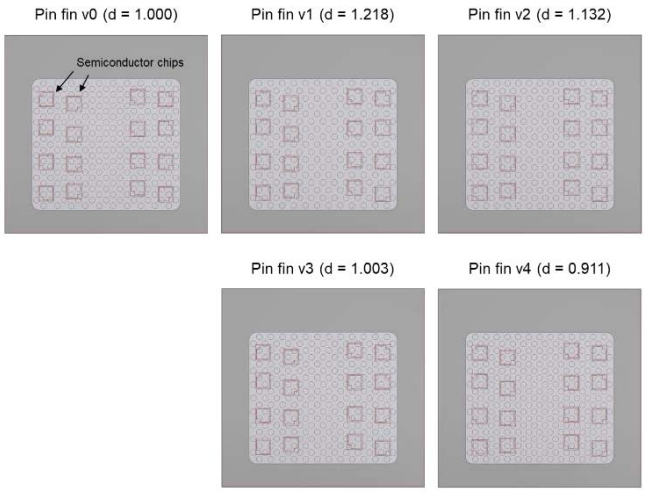

Fig. 3: Different pin fin distributions considered for parallel configurations (chip positions shown for reference in red). Parameter d represents the minimum distance between pins, in mm.

In order to obtain a fair comparison between cooling schemes, four additional pin fin layouts (*pin fin v1 .. v4*) with optimized structure specifically for the case of parallel cooling were compared against the corresponding optimized layout for serial cooling (*pin fin v0*). All simulated pin fin layouts can be seen in Fig. 3.

For the creation of these additional geometries, base plate manufacturing design rules were considered, and the comparison also included an unrealizable case (*pin fin v4*) for a complete understanding.

- **Scenario 3: Parallel configuration using meander channels**

Power modules with meander configuration of the coolant channels absorbed market attention in recent years and were therefore considered in this study for benchmarking purposes. For a fair comparison, the outer dimensions of *surface A* in Fig. 2 were left unchanged.

In this framework, six meander cooling structures were modeled using different values for the following parameters: fluid by-pass between the edge of the module and the cooler (from 0.2 mm to 0.6 mm), opening between channels (from 3 mm to 4 mm), radius of edges (from 0.3 mm to 0.5 mm) and height of the structures (short version of 3 mm and long version of 8.2 mm).

For all versions, three channels with 11 intermediate turns per channel were used, and the meander turns were modeled using a radius of 2.8 mm. In all cases, the thickness of the walls forming the structures were 1 mm thick.

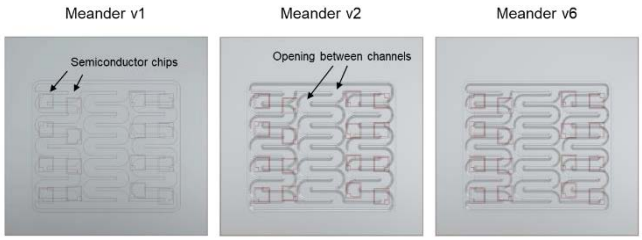

Fig. 4: Meander channels considered for parallel configurations (chip positions shown for reference in red). Additional simulated cases (*v3, v4, v5*) are not shown as geometrical changes are not noticeable from the selected view.

CFD simulations using COMSOL Multiphysics were performed for each case, considering the same boundary conditions for a fair comparison: ethylene glycol – water 1:1 mixture coolant, flow

rate Q = 10 L/min and temperature of the coolant at the inlet of the cooler T_a = 65ºC.

In order to validate the thermal simulation results, several experiments with a thermal imaging camera were performed at HAPG Semiconductors using the standard RoadPak module.

3 Results and discussion

3.1 CFD simulations

The thermal results shown in Fig. 5 exhibit the thermal resistance per module side ($R_{th\,j-a}$) of the hottest chip junction with respect to T_a for the aforementioned cooling condition.

For the RoadPak module with pin fin cooling structures in serial configuration, the $R_{th\,j-a}$ is 18% lower than the best case using pin fin geometry in parallel configuration (*pin fin v0*).

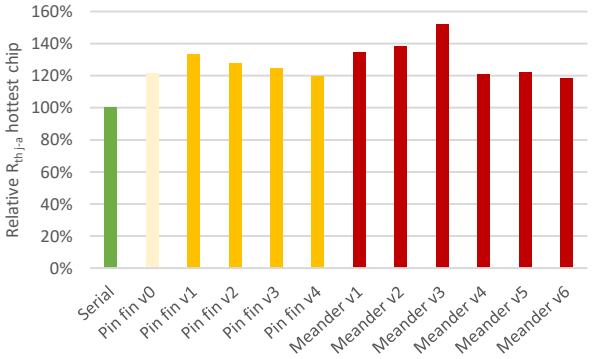

Fig. 5: Relative $R_{th\,j-a}$ of the considered cases. Serial cooling with pin fin in green, parallel pin fin in yellow (original pin fin structure in light yellow) and parallel meander in red.

Note that *pin fin v4*, while having slightly better thermal results than *pin fin v0*, is not considered as optimal because its manufacturability in high volume is not realizable with existing cost-effective manufacturing methods in the market.

When comparing the serial configuration using current pin fin design against the meander structures considered in this study, the results showed that the serial configuration yields a 16% lower $R_{th\,j-a}$ than the best meander structure in terms of thermal performance (*meander v6*).

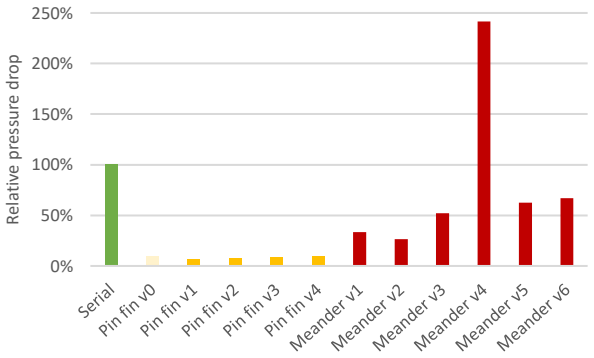

Fig. 6: Relative pressure drop of all considered cases. Color legend according to Fig. 5.

Regarding Δp results (see Fig. 6), the parallel concept with pin fin yields a 90% lower Δp than the serial pin fin, while, for the parallel meander distribution, the Δp decrease is only 38% for the best thermal performance version (*meander v6*).

The outlier high Δp value (*meander v4*) can be explained by a shorter meander channel geometry (3 mm high compared to 8.2 mm in other cases)

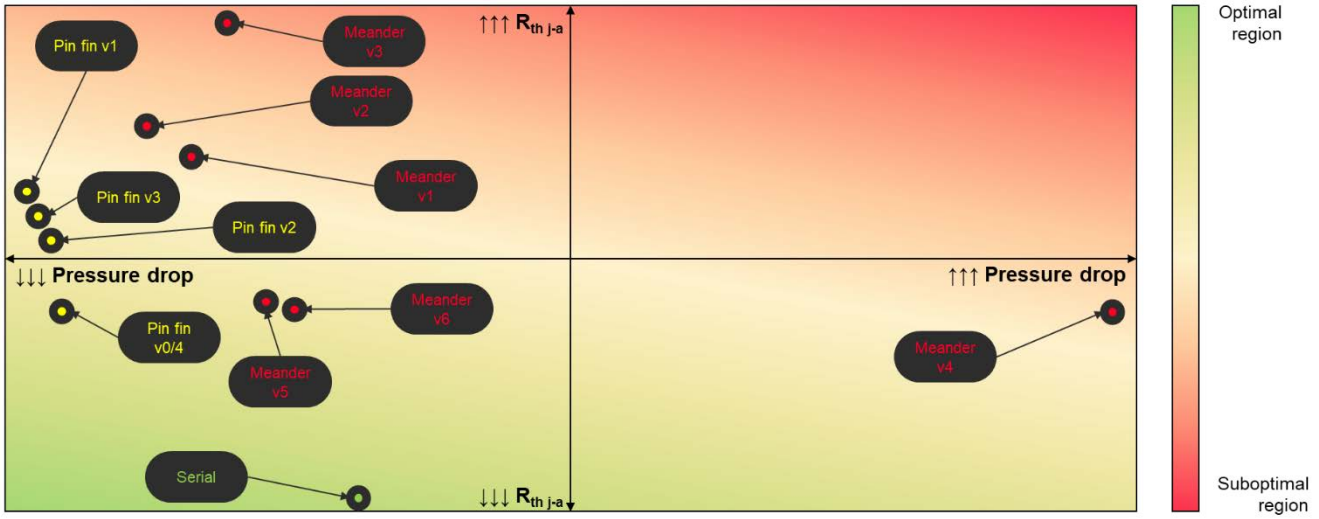

Fig. 7: Relative $R_{th\,j-a}$ of the considered cases. Serial cooling with pin fin in green, parallel pin fin in yellow (original pin fin structure in light yellow), parallel meander in red.

ISBN 978-3-8007-5515-8

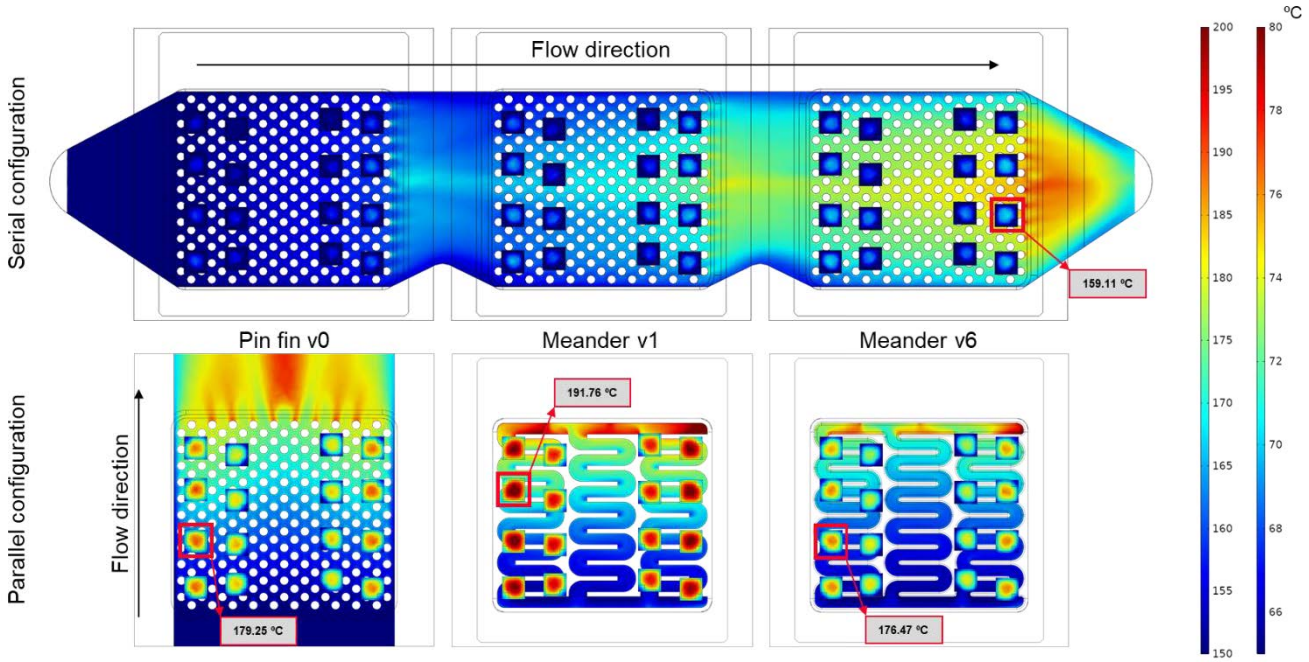

Fig. 8: Temperature contours at chip junction (left temperature scale) and at horizontal cut plane at coolant region (right temperature scale). Average temperature of hottest chip for each case shown for reference in red squares.

combined with a very small by-pass (200 µm compared to 600 µm in other cases).

By combining the thermal performance and pressure drop results, it can be inferred that both pin fin and meander structures can achieve similar $R_{th\,j-a}$ values (Fig. 7). However, the usage of pin fin structures is much more pressure drop effective (between 3 and 7 times less). The reason for this is that, for a given Q, the velocity of the coolant inside the structures is considerably lower for the pin fin cases than for the meander cases, due to a bigger channel flow cross-section of the pin fin cases compared with the meander cases.

The CFD results also showed the effect of the heating of the coolant when the modules are cooled in serial or in parallel (see Fig. 8). Due to a higher flow rate felt by the modules in the serial cooling configuration, the coolant heating below a single module was, in average, 3 times smaller than the coolant heating per module in parallel cooling configurations. This phenomenon is especially relevant for a low-temperature coolant scenario, given the increase in viscosity faced by the coolant (typically, a mixture of ethylene-glycol-water with 1:1 ratio), which decreases the applicable flow rate that the pump can provide to the system, enlarging the coolant temperature increase. A high temperature increase per module can lead to substantially unequal chip temperatures, which can affect the current distribution during operation, leading to reliability issues and reduced lifetime.

In terms of chip junction temperature, Fig. 8 highlights the differences between different cooling configurations, and the location of the hottest chip in each of them. As already stated, the serial cooling configuration with pin fin structures provides the coldest chip temperatures.

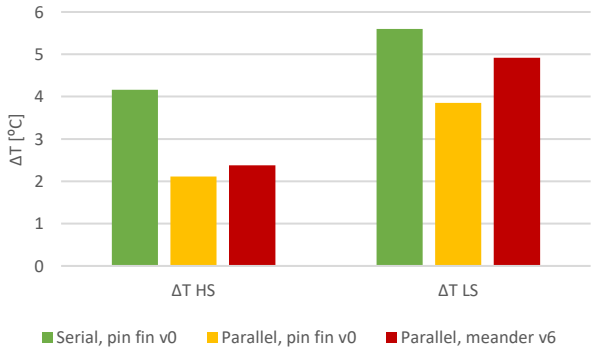

Fig. 9: Temperature difference between hottest and coldest chip junctions for HS and LS in the considered cooling scenarios.

However, when looking at temperature distribution within a single module (see Fig. 9), parallel pin fin configurations show the lowest temperature

ISBN 978-3-8007-5515-8

differences between hottest and coldest chips for both high side (HS) and low side (LS), followed by parallel meander configurations and finally serial configurations, which presented the highest difference.

As briefly explained before, a module with an excessive temperature difference between hottest and coldest chip can potentially provoke an imbalance in the current share per chip. For this reason, a steady-state electro-thermal simulation of a RoadPak module with serial cooling configuration powered with a DC current of 550 A was performed to monitor the current share per chip. In contrast to previously shown cases, the simulated module, shown in Fig. 10, had 10 chips per side (vs 8) to match the experiment described in section 3.2.

In order to capture the temperature effect on the current sharing, the electrical conductivity of the chips was considered temperature dependent and derived from $R_{DSon}(T)$ measurements taken on module level at HAPG Semiconductors.

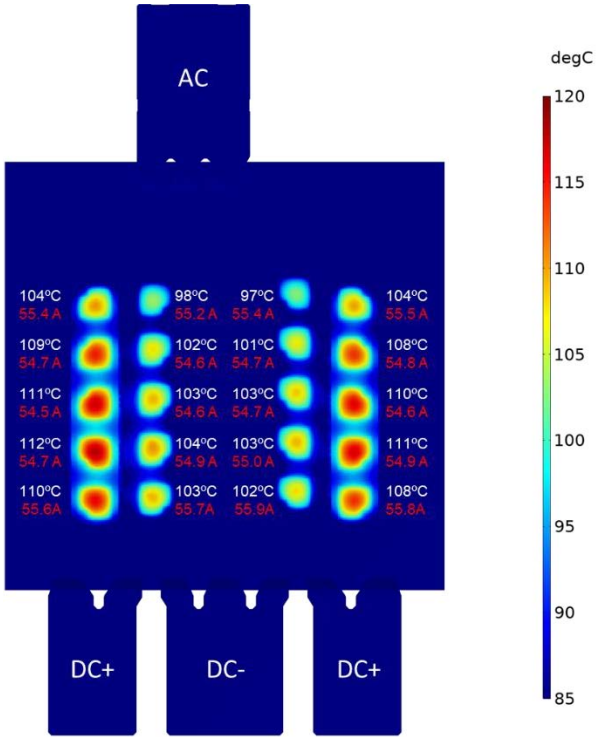

Fig. 10: Temperature contour of electro-thermal simulation with RoadPak module with 20 chips applying a DC current of 550 A.

The simulation results show a very balanced current sharing, with a max-min slightly higher than 1 A, which corresponds to less than ±1% of variation between most and less conductive chip, demonstrating the low effect of temperature differences between SiC chips on a HAPG RoadPak module.

3.2 Experiment validation

Several experiments were performed on a black-sprayed open module (no mold compound encapsulation) built with R_{DSon}-balanced chips with the purpose of validating the $R_{th\,j-a}$ results obtained from simulations. The tests were carried out on a power cycling tester at HAPG Semiconductors and the temperature over time was measured with the use of a calibrated thermal imaging camera.

A DC current of 550 A was applied during the heating up phase (60 s), while for the cooling down phase (60 s) there was no current applied. A coolant mixture of ethylene glycol and water (1:1) at a constant flow rate of 10 L/min was used for heat dissipation. The coolant temperature at the cooler inlet was 20ºC.

The temperature of each chip was analyzed over time considering the average temperature of the areas marked in Fig. 11, avoiding probing wire bonds.

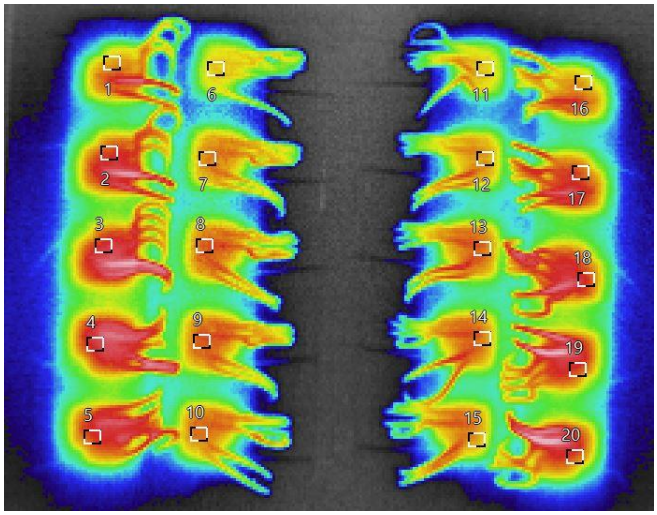

Fig. 11: Infrared thermography of a RoadPak module assembled without mold compound during experiments carried out at HAPG Semiconductors. Both HS and LS chips are powered with a DC current of 550 A.

The temperature results obtained from these experiments showed reasonable agreement between the measured $R_{th\,j-a}$ of every chip and the simulation results with the same boundary conditions, yielding an average precision of approximately 10%.

ISBN 978-3-8007-5515-8

The use of adiabatic boundary conditions for all surfaces not in contact with the coolant can explain the higher temperature values obtained from the simulation, not considering effects such as the conduction of the module to the clamping system or the convection and radiation heat transfer occurring at the module surface.

In absolute terms, the $R_{th\,j-a}$ values of the RoadPak module showed outstanding thermal performance. This is a combined effect of detail-optimized cooling structures, substrate design and chip layout, allowing the RoadPak module to switch fast and reliably during operation [5].

The low thermal resistance allows the RoadPak module to achieve high levels of current rating. In this regard, for selected high-demanding applications such as Formula E, it is possible to increase the current rating of the module in different ways, among them increasing the thermal performance of the module [6].

4 Conclusions

Our study reveals that, in the framework of the RoadPak module, a serial cooling configuration of optimized pin fin structures provides the best thermal results at a good compromise with pressure drop requirements for typical nominal conditions.

Firstly, serial configurations yielded lower temperature increase and, therefore, lower $R_{th\,j-a}$ values for the hottest chip of the module. This allows a higher current rating than the one achievable by the same module in parallel cooling configurations.

Secondly, optimized pin fin configurations and meander configurations showed comparable thermal performance. However, the provoked pressure drop is considerably higher for meander than pin fin configurations.

Additionally, simulation temperature results were validated performing several experiments on a balanced open module, which showed a good agreement between the two methodologies and confirmed the outstanding low thermal resistance of the package.

Considering these findings, the RoadPak module is built on an optimized pin fin base plate and is assembled on a serial configuration for all forecasted eMobility applications.

5 References:

[1] J. Schuderer, C. Liu, N. Pavlicek, G. Salvatore, J. Loisy et al., “High-Power SiC and Si Module Platform for Automotive Traction Inverter”, PCIM Europe, Nürnberg, Germany, May 2019

[2] C. Liu, Y. Chao, S. Yang, R. Fang, W. Han et al., "Direct liquid cooling For IGBT power module," 2014 9th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), Taipei, 2014, pp. 41-44

[3] J. Schulz-Harder, K. Exel and A. Meyer, "Direct Liquid Cooling of Power Electronics Devices," *4th International Conference on Integrated Power Systems*, Naples, Italy, 2006, pp. 1-6.

[4] T. Gradinger and D. Torressin, “Pin-fin design and optimization for direct cooling of electric-vehicle traction inverters”, PCIM Europe, Nürnberg, Germany, May 2019

[5] A. Mesemanolis, M. Maleki, S. Hartmann, A. Ruiz, D. Weiss et al., “Fast and Reliable Switching of Parallel SiC MOSFET Chips in a Half-Bridge Module”, PCIM Europe, Nürnberg, Germany, May 2020

[6] M. Maleki, A. Mesemanolis, L. Santolaria, A. Ruiz and T. Keller, “High power density SiC power module for Formula E: requirement, design considerations and the test results”, PCIM Europe, Nürnberg, Germany, May 2021