

SiC Application Note

Application Benefits of Using 4th Generation SiC MOSFETs

[Abstract] In electric vehicles (EVs), data centers, base stations, smart grids, etc., the voltage and capacity of power sources are increasing because they can enhance the convenience of people's lives. However, from the viewpoint of global environmental conservation efforts, it has become more and more important not only to improve convenience but also to reduce the losses of the power converter and use it effectively. Therefore, attention is being paid to SiC power semiconductors that can operate at high frequencies, withstand high voltages and operate at high current densities. All this with low energy loss. ROHM has released the 4th generation of SiC MOSFETs, which has evolved from the existing trench gate structure. It has achieved a 40% reduction in on-resistance and a 50% reduction in switching loss compared to the 3rd generation. In this application note, an experimental test using a step-down DC-DC converter with 500V input voltage and 7kW power, a simulated running test using an EV traction inverter with 800V input and 100kW, and an experimental test using a Totem-pole PFC circuit were conducted. We confirmed its usefulness and benefit.

1. Introduction
2. 4th Generation SiC MOSFET in Step-down DC-DC Converter
 - 2.1 Circuit Operation Principle and Theoretical Analysis of Loss
 - 2.2 Experimental Verification of DC-DC Converter
3. EV application
 - 3.1 Simulated Driving Test with Traction Inverter
 - 3.2 Evaluation of Totem-pole PFC
4. Summary

1 Introduction

Today, applications such as electric vehicles (EVs), data centers, base stations, smart grids, etc. are progressing toward higher voltage and higher power levels (Figure 1). The reason for this is that it can enhance the convenience of each application. In the case of EVs, for example, higher voltages (400V or 800V) and higher power (up to 350kW) can extend the cruising range and shorten the charging time through quick charging, which will greatly enhance the convenience of people's lives. However, as the world is currently strengthening its efforts to protect the global environment, simply improving comfort will not be enough to gain acceptance in the global market. In the future, in addition to improving convenience, it will become increasingly important to reduce energy loss and use it effectively. The key point to focus on is power conversion. In all the aforementioned applications, power is supplied from the power grid, batteries, solar power generation systems, etc., and converted to the optimal voltage for effective use. In order to reduce energy loss and increase power conversion efficiency, SiC power semiconductors are currently attracting attention for their ability to operate at high frequency, high voltage and high current density with low energy loss. ROHM has already commercialized SiC power semiconductors, which are used in a variety of applications

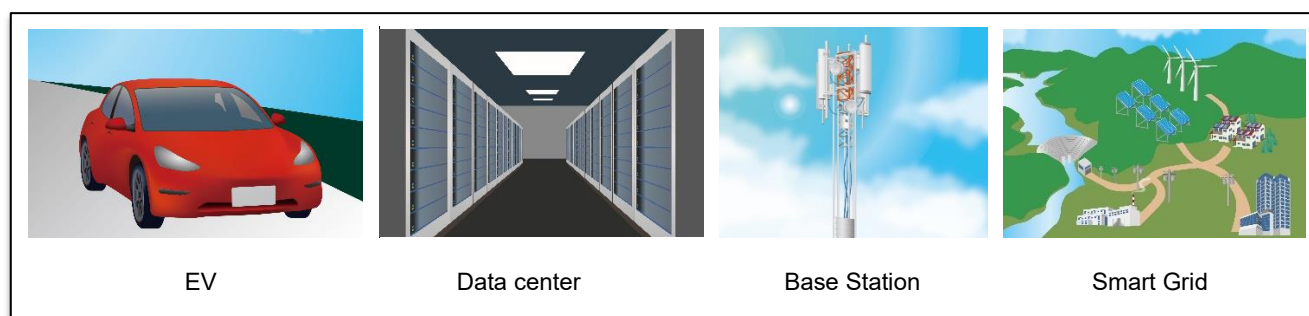


Figure 1. Application examples

ROHM has released the 4th Generation of SiC MOSFETs. By further evolving the trench gate structure established in the 3rd generation SiC MOSFETs already in mass production, ROHM has reduced on-resistance by approximately 40% and switching loss by approximately 50% due to high-speed switching characteristics compared to the 3rd generation. This evolution is shown in the trend of normalized on-resistance (Ron-A: on-resistance per unit area) shown in Figure 2.

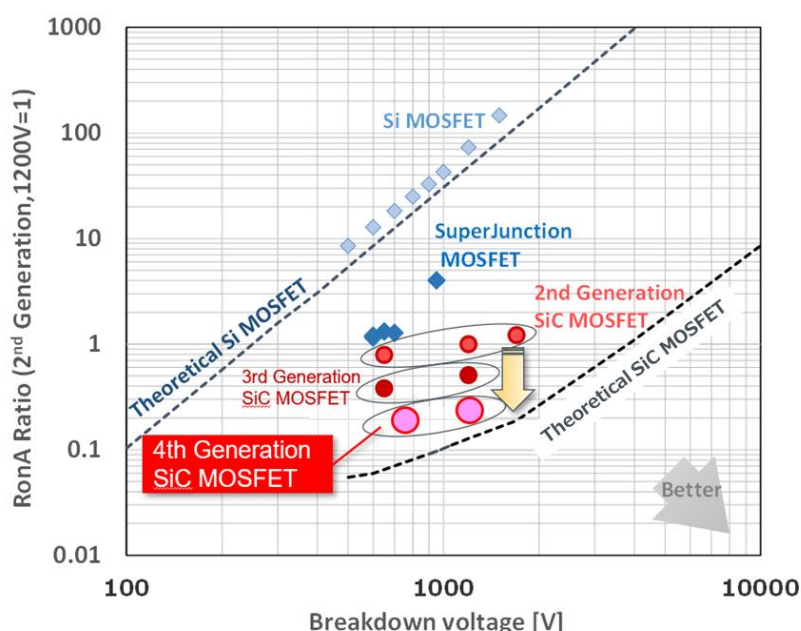


Figure 2. Trend Graph of Normalized On-resistance

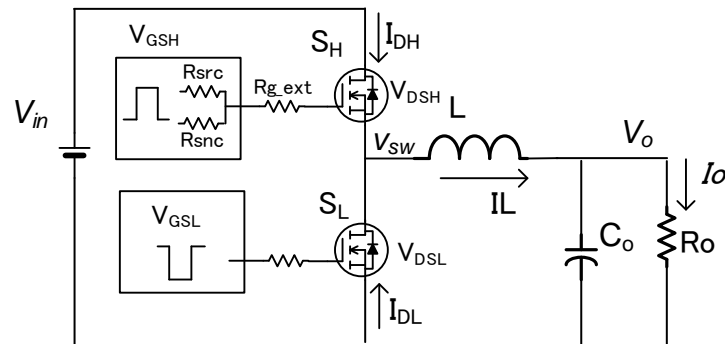
In this application note, Chapter 2 describes how 4th Generation SiC MOSFETs contribute to the improvement of converter efficiency in a basic buck DC-DC converter. The mechanisms of switching loss, conduction loss, body diode loss, recovery loss, etc. are explained, and the effect of loss reduction when 4th Generation SiC MOSFETs, which excel in fast switching, are used in converters is illustrated.

Chapter 3 describes a power solution for EVs as a specific application example, where the EV power conversion consists of on-board chargers (OBCs), isolated DC-DCs for auxiliaries, boost DC-DCs, and motor traction inverters. In particular, the motor traction inverter will be simulated using a motor test bench to explain how the characteristics of the 4th Generation SiC MOSFETs can benefit the user. It will also be explained how the Totem-pole PFC, which is as a part of the OBC, will also benefit from the 4th generation SiC MOSFETs.

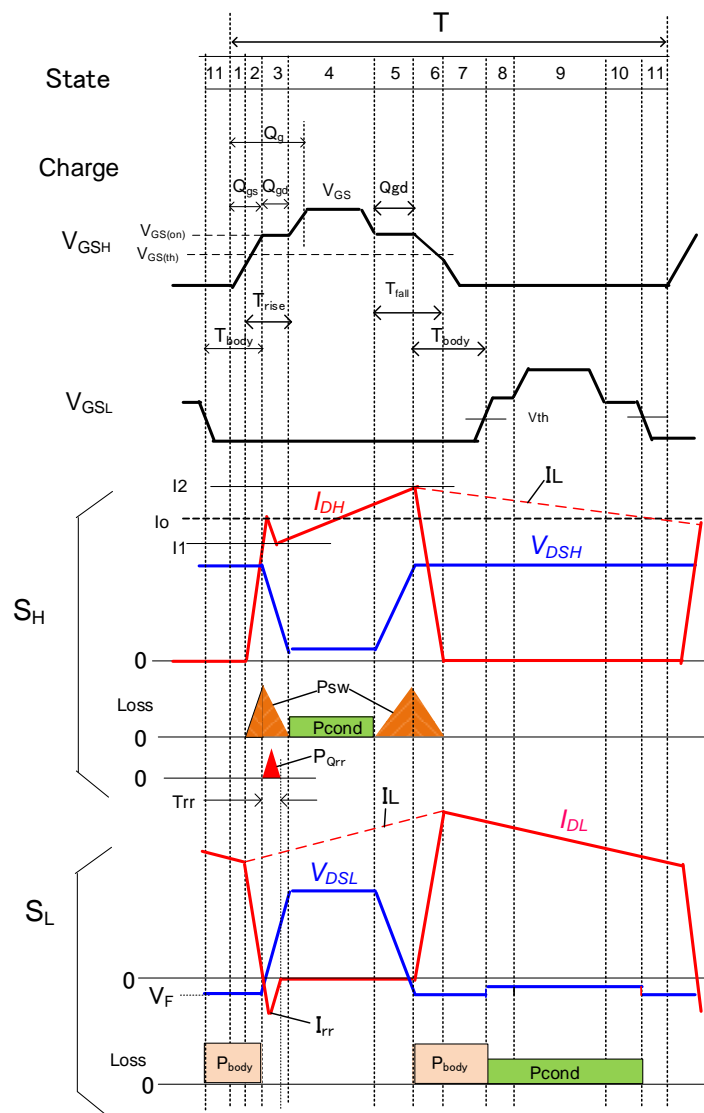
2. 4th Generation SiC MOSFET in Step-down DC-DC converter

2.1 Circuit Operation Principle and Theoretical Analysis of Loss

In contrast to the 3rd generation SiC MOSFETs, the 4th generation SiC MOSFETs offer improved switching speed, which contributes significantly to lower switching losses. Figure 3(a) shows the block diagram of the buck converter and Figure 3(b) shows the general switching waveforms of the converter.



(a) Step-down DC-DC converter Block diagram



(b) Key switching waveforms

Figure 3. Step-down DC-DC Converter (half bridge)

As shown in Figure 3(b), power device losses in a converter consist of switching losses, conduction losses, body diode losses, recovery losses, and C_{oss} losses. (C_{oss} loss is omitted from the figure because it is small.)

As for switching loss, it is generally described in the datasheet as energy per E_{on} and E_{off} pulse, which is a useful for loss estimation in the initial design stage. In detailed design, it is necessary to strictly determine the power dissipation at high voltage input and high frequency. The gate driving circuitry has a large impact in the device losses, so optimizing the gate drive design is necessary to take advantage of the high-speed switching characteristics of SiC devices.

The switching loss occurs only in the high-side FET (S_H) and is expressed by equation (1).

$$P_{sw} = \frac{1}{2} V_{in} I_1 T_{rise} f_{sw} + \frac{1}{2} V_{in} I_2 T_{fall} f_{sw} \quad (1)$$

In State 1, the gate voltage V_{GS} is applied to the SiC MOSFET of the high-side FET (S_H). When the gate voltage exceeds the threshold $V_{GS(th)}$ in State 2, the inductor current starts to flow rapidly in the channel of S_H and reaches the load current I_o in only a few ns until $V_{GS(on)}$ (plateau voltage). Then, during the State 3 (plateau period), the channel turns on and V_{DS} reaches zero volts. This period between State 2 and State 3 is the switching period T_{rise} at turn-on shown in equation (2). In this equation, the amount of charge in State 2 is usually not described in the data sheet, so it is estimated from Q_{gs} and adjusted by setting the coefficient as k (k is usually $1/3$ - $1/4$). The gate current, I_{g_on} , is determined by the potential difference between the gate driver voltage, V_{GS} , and the gate on voltage, $V_{GS(on)}$, and the intervening resistance, and is given by equation (3). In this equation, R_{src} is the source resistance of the gate driver, R_{g_ext} is the external gate resistance, and R_{g_int} is the internal gate resistance of the SiC MOSFET.

$$T_{rise} = \frac{\frac{1}{k} Q_{gs} + Q_{gd}}{I_{g_on}} \quad (2)$$

$$I_{g_on} = \frac{V_{GS} - V_{GS(on)}}{R_{src} + R_{g_ext} + R_{g_int}} \quad (3)$$

(State 4 will be explained later).

During State 5-6, the gate voltage drops and the device enters the turn-off state. This T_{fall} period is represented by equation (4). It is important to note that the gate current I_{g_off} during the T_{fall} period has a numerator of $V_{GS(on)}$ only, as shown in equation (5). In general, the turn-off time is slightly longer. In the equation, R_{snk} is the sink resistance.

$$T_{fall} = \frac{\frac{1}{k} Q_{gs} + Q_{gd}}{I_{g_off}} \quad (4)$$

$$I_{g_off} = \frac{V_{GS(on)}}{R_{snk} + R_{g_ext} + R_{g_int}} \quad (5)$$

In the case of a constant current source such as an inductor load, the current waveform I_D and voltage waveform V_{DS} do not overlap in the timing of change, so the switching loss P_{sw} in equation (1) has a factor of $1/2$.

Also, during the T_{rise} period, the charge stored in the drain-source capacitance C_{ossH} is short-circuited in the channel, resulting in a charge-discharge loss P_{cosH} (Equation (6)).

$$P_{cosH} = \frac{1}{2} C_{cosH} \cdot V_{in}^2 \cdot f_{sw} \quad (6)$$

In State 4, the conduction loss P_{condH} occurs during the period when the high-side FET (S_H) is completely on (Equation (7)). The effective current at that time is given by equation (8) using the time ratio D ($=V_o/V_{in}$).

$$P_{condH} = I_{S_H-rms}^2 \cdot R_{DS(on)} \quad (7)$$

$$I_{S_{H_rms}} = \sqrt{D \left(I_o^2 + \frac{\Delta I_L^2}{12} \right)} \quad (8)$$

These are switching loss, conduction loss, and C_{oss} loss generated in the high side FET (S_H).

The subsequent states are the losses that occur in the low-side FET (S_L).

State 7, State 11 and State 1 are dead time periods. The loss is generated by the current conducted through the body diode of the low-side FET (S_L) (Equation (9)).

$$P_{body} = I1 \cdot V_F \cdot T_{dead1} \cdot f_{sw} + I2 \cdot V_F \cdot T_{dead2} \cdot f_{sw} \quad (9)$$

In State 8-10, the conduction loss of the low-side FET (S_L) occurs (Equation (10)). At that time, the effective current is given by equation (11).

$$P_{cond_L} = I_{S_{L_rms}}^2 \cdot R_{DS(on)} \quad (10)$$

$$I_{S_{L_rms}} = \sqrt{(1 - D) \left(I_o^2 + \frac{\Delta I_L^2}{12} \right)} \quad (11)$$

The charge/discharge loss of C_{oss} in the low-side FET (S_L) is usually ignored because the charge of C_{oss} is already discharged by the inductor current I_L when S_L turns on (State 8), resulting in ZVS (Zero Voltage Switching).

These are the losses that occur in the low-side FET (S_L).

Here is the explanation of the recovery loss P_{Qrr}. The timing of the loss is State 3, and it is caused by the recovery of the body diode of the low-side S_L (Equation (12)). This loss is shared by the high-side FET (S_H) and the low-side FET (S_L), but for simplicity, we will integrate it into the high-side.

$$P_{Qrr} = 0.5 \cdot V_{in} \cdot Q_{rr} \cdot f_{sw} \quad (12)$$

From the above, the total loss of the high-side FET (S_H) and low-side FET (S_L) is given by equations (13) and (14), respectively.

$$P_{S_H} = P_{sw} + P_{cond_H} + P_{coss_H} + P_{Qrr} \quad (13)$$

$$P_{S_L} = P_{cond_L} + P_{body} \quad (14)$$

In particular, regarding switching loss, equations (2) and (4) show that the smaller the Q_{gd} (the charge of the gate-to-drain capacitance C_{rss}), the shorter Trise and Tfall times will be, which leads to the lower switching loss P_{sw} in equation (1). The 4th generation SiC MOSFET has reduced this Q_{gd} by about half compared to the 3rd generation MOSFET, which significantly cuts down the switching losses. This is effective in reducing losses where the switching frequency of the converter is high, and in the EV application which is often operated with a light load on average. This results in longer cruising range and lower running costs. This is a major advantage of using 4th generation SiC MOSFETs.

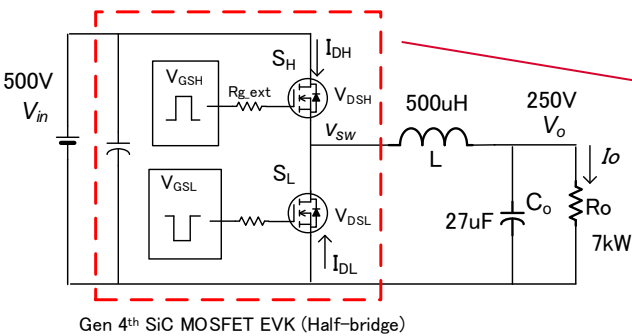
2.2 Experimental Verification of DC-DC Converter

In order to confirm previous analysis, we incorporated the 4th Gen SiC MOSFETs into a step-down DC-DC converter with the following specifications and verified it experimentally with an evaluation board.

Figure 4 shows (a) the DC-DC converter circuit and (b) the evaluation board for the 4th generation SiC MOSFETs used in the half-bridge section with built-in decoupling capacitor. The inductor L, output capacitor Co, and input bulk capacitor are external.

Table 1 Specifications of DC-DC Converters and SiC Device

V _{in}	500V
V _o	250V
P _o	7kW
f _{sw}	50kHz
L	500uH
R _{g_ext}	3.3ohm
4 th Generation SiC MOSFETs	SCT4036KR 1200V/36mΩ
3 rd Generation SiC MOSFETs (as a reference)	SCT3040KR 1200V/40 mΩ



Gen 4th SiC MOSFET EVK (Half-bridge)

(a) DC-DC converter block diagram for test



(b) 4th generation SiC MOSFET EVK (Half-bridge)

Figure 4. DC-DC Converter Block Diagram for Test and 4th Generation SiC MOSFET EVK

Figure 5 shows the V_{GS} , V_{DS} , and I_D waveforms at 50 kHz during turn-on and turn-off. The turn-on waveform is enlarged on the left. From the waveform observation, we can see that the turn-on rise time T_{rise} is about 20ns, which is very fast. Figure 6 shows the measurement results of efficiency and power dissipation of this DC-DC converter. Figure 6 shows the efficiency and loss of the DC-DC converter. At light loads (around 1kW), the low switching loss, which is a characteristic of the 4th generation SiC MOSFET, is presented. Figure 7 shows the results of the theoretical analysis of the loss breakdown as a converter. Figure 7 shows the theoretical analysis of the loss breakdown as a converter. It shows that the loss is improved by about 15W, and especially the switching loss of the high-side FET (S_H) and the recovery loss P_{Qrr} are greatly reduced, which contributes to the improvement of the overall loss.

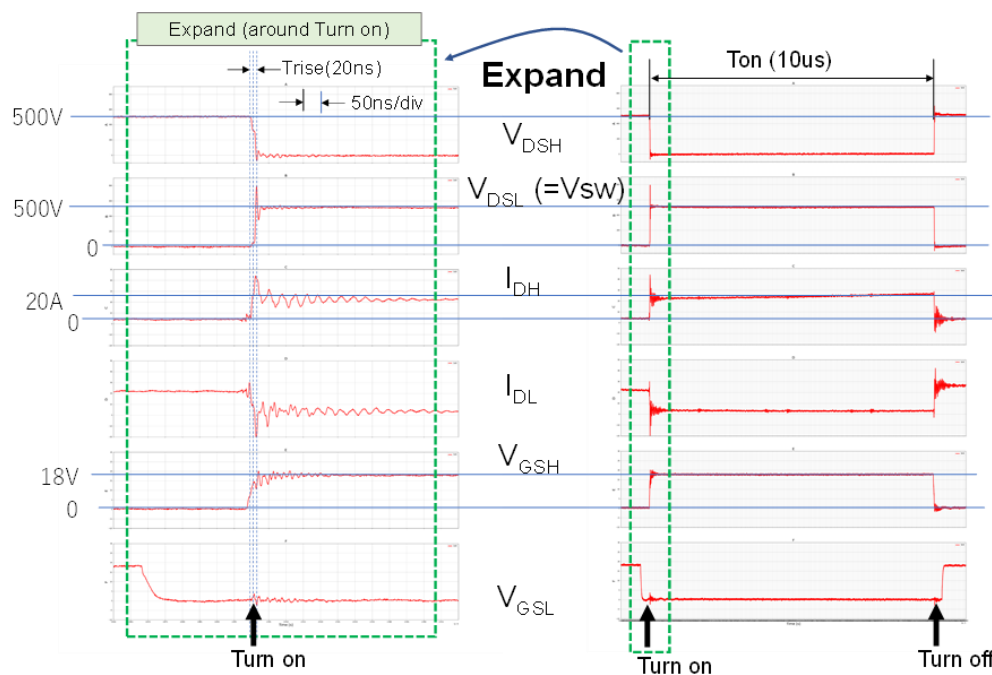


Figure 5. Observed Switching Waveforms (500Vin, 250Vo/20A(5kW), 50kHz)

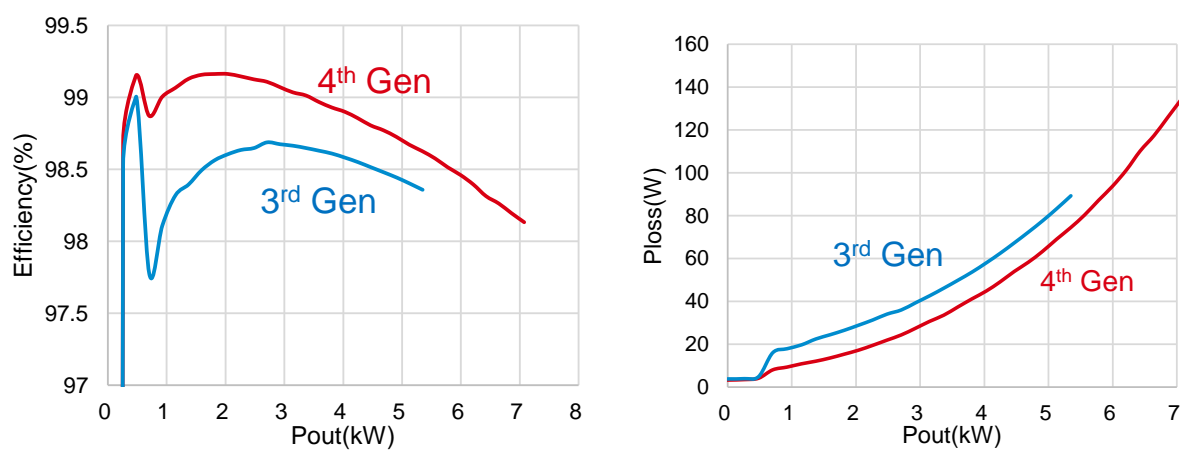


Figure 6. Measured Efficiency and Losses (500Vin, 250Vo/7kW)

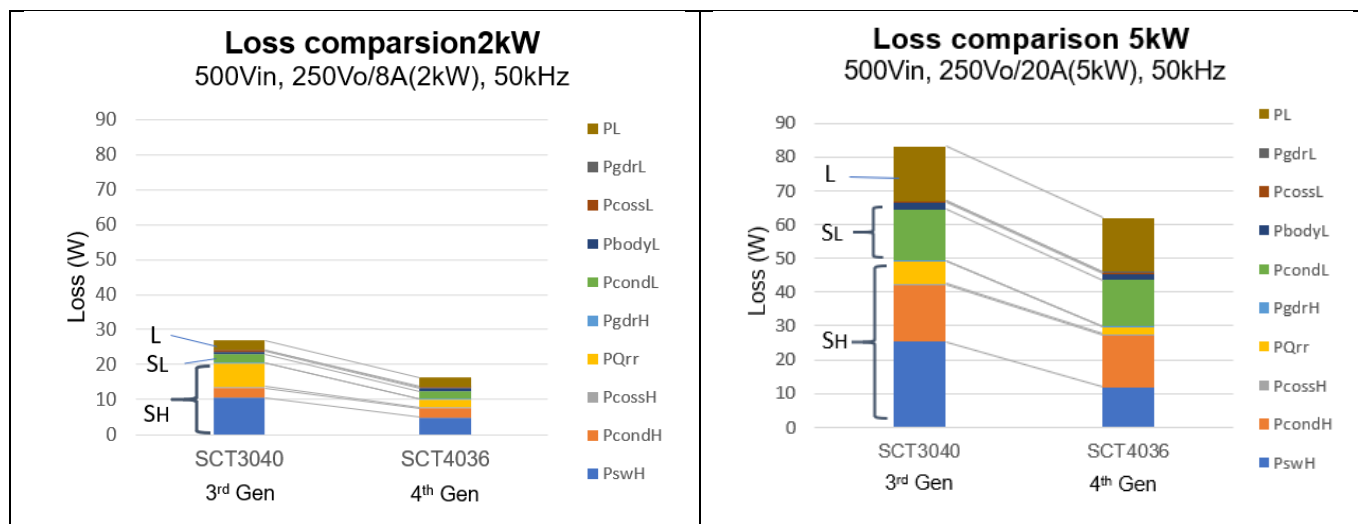


Figure 7. Calculated Loss Analysis (Left : 2kW, Right : 5kW)

3 EV Application

There are various types of EVs, such as BEVs, HEVs, PHEVs, and series HEVs, with different power architectures for different applications, as shown in Figure 8. Among them, the power architecture of BEVs with 400V or 800V battery voltage supporting bi-directional and fast charging has been attracting attention recently.

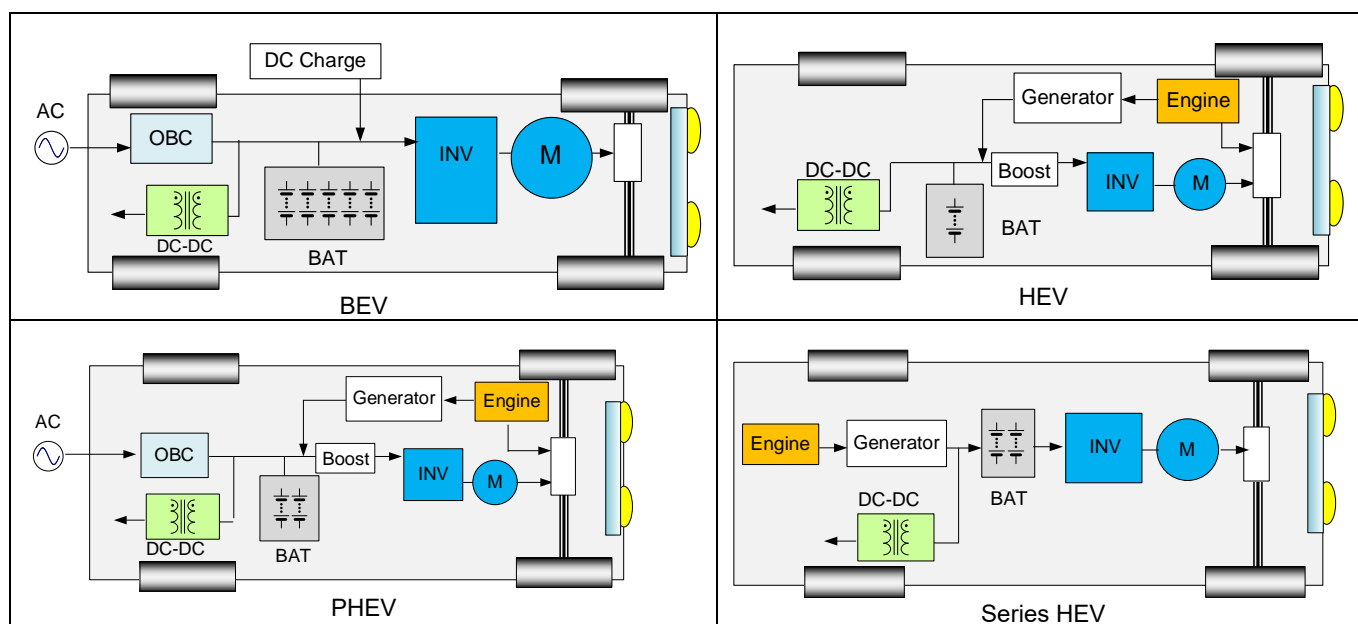


Figure 8. Various Types of EVs

Figure 9 shows a block diagram of the BEV power architecture as an example: the OBC (On-Board Charger) is a hot topic topology with bi-directional Totem-pole PFC and bi-directional CLLC (Symmetric LLC), assuming V2G (Vehicle To Grid). From the output of this OBC, power is supplied to the auxiliary DC-DC converter, the battery, the boost converter to the inverter and the motor traction inverter.

Chapter 3.1 describes the basic operation of the traction inverter and the evaluation system (motor test bench test environment) in an EV. Chapter 3.2 describes the experimental results of using 4th Generation SiC MOSFETs in an OBC bi-directional totem-pole PFC. In chapter 3.2, the experimental results of using 4th Generation SiC MOSFETs in an OBC bi-directional totem-pole PFC are presented.

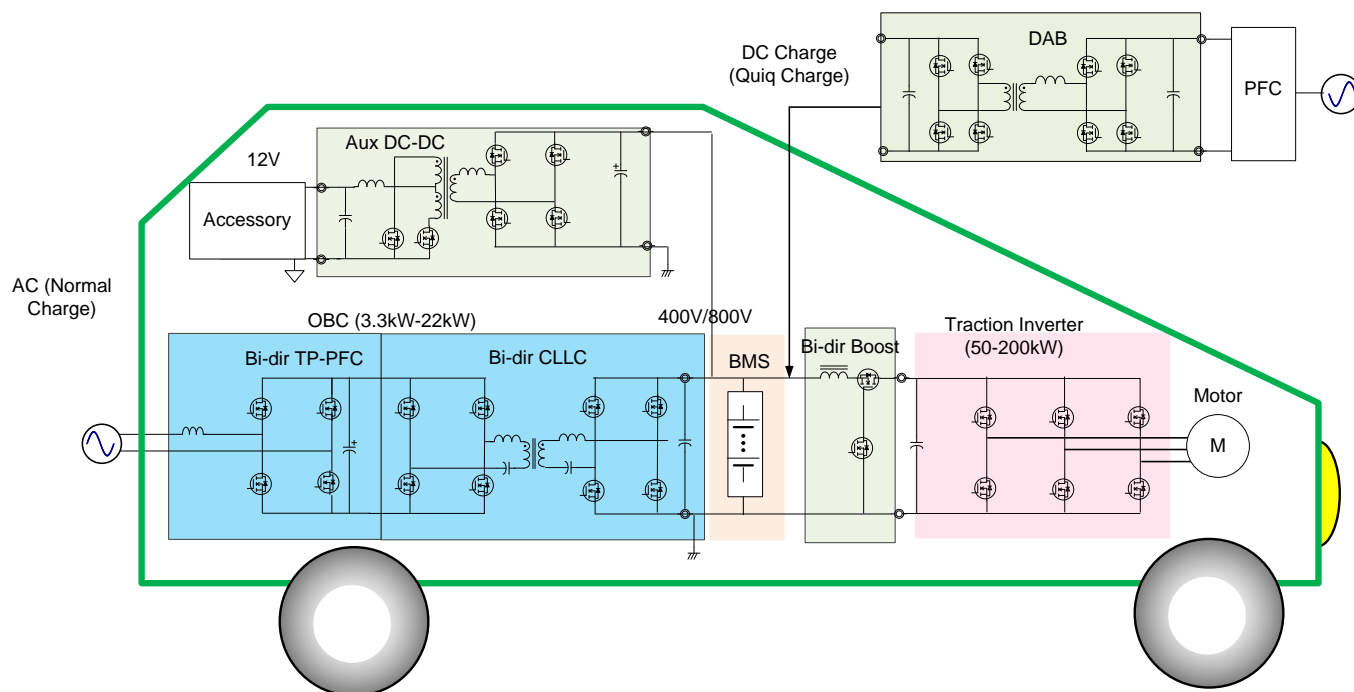


Figure 9. An example of BEV Power Architecture

3.1 Simulated Driving Test with Traction Inverter

[1] Inverter Circuit Operation

As the integration of mechanical and electrical components (motors, reduction gears, and inverters) continues to progress, the importance of reducing losses in order to achieve high voltage, high output, compact, and lightweight inverters is increasing. This is because it directly affects the cost performance of EVs.

As shown in Figure 10, the traction inverter converts the DC power provided by the battery into 3-phase AC power to drive the motor in the powertrain. The three-phase AC waveform is set by a signal wave (reference sine wave) with a frequency synchronized with the motor speed, and a triangular wave (modulation wave) with a carrier frequency that determines the switching frequency. The voltage supplied to the motor is determined by changing the levels of the 3-phase AC and triangular waves when generating the PWM signal.

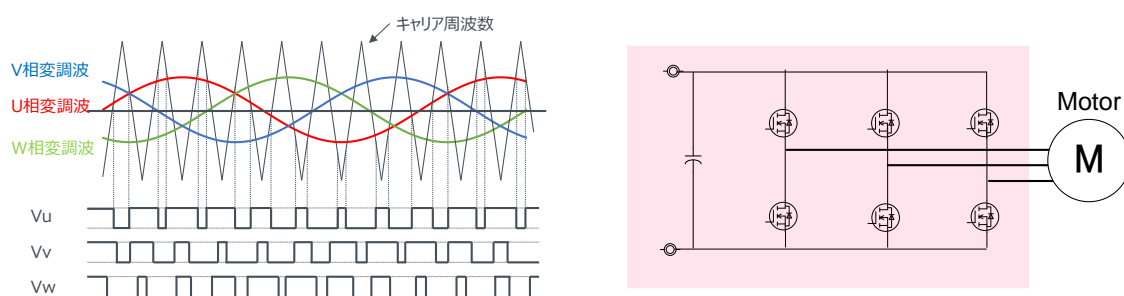


Figure 10. Inverter Circuit Configuration and Drive Signal

[2] Motor Test Bench Environment

Table 2 shows the main specifications of the SiC devices installed in the motor test bench and the DUT inverter. The DUT inverter consists of a 2-in-1 power module with a 4th generation SiC MOSFET bare chip.

Figure 11 shows the test environment of the motor test bench, Figure 12 shows the DUT inverter, and Figure 13 shows the

control system block diagram. The test motor is driven from the DUT inverter through a 3-phase uvw power line. The test motor is connected to the load motor, and the load motor is controlled by the load torque according to the running resistance calculated from the vehicle parameters, which enables the simulated running experiment with the desired vehicle parameters. Here, as shown in Figure 14 and equations (15)-(18), the running resistance takes into account the air resistance F_{AD} , rolling resistance F_{RR} , gradient resistance F_{RG} , and acceleration resistance F_{ACC} .

Table 2. Main specifications of motor test bench and test inverter

DC power supply	capacity	100kW
	Output voltage range	0 to 850V
	Output current range	$\pm 500A$
Test motor	Type	PMSM
	Rated output	100kW
	Maximum torque (1 minute)	350Nm
	Cooling method	Water cooling
Test inverter	Power module	4 th generation SiC MOSFET 1200V/400A
	Switching frequency	10kHz
	Cooling method	Water cooling
Cooling water circulation device	Cooling temperature range	20 to 90 deg.C
	Refrigerant	Ethylene glycol aqueous solution

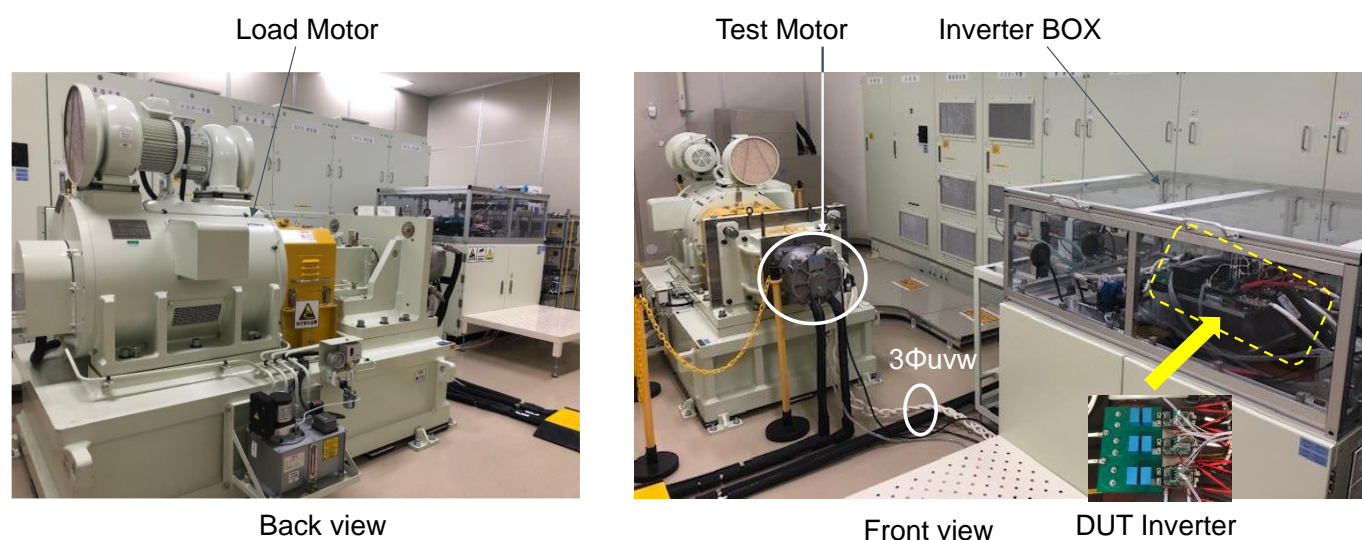


Figure 11. Motor Test Bench Environment

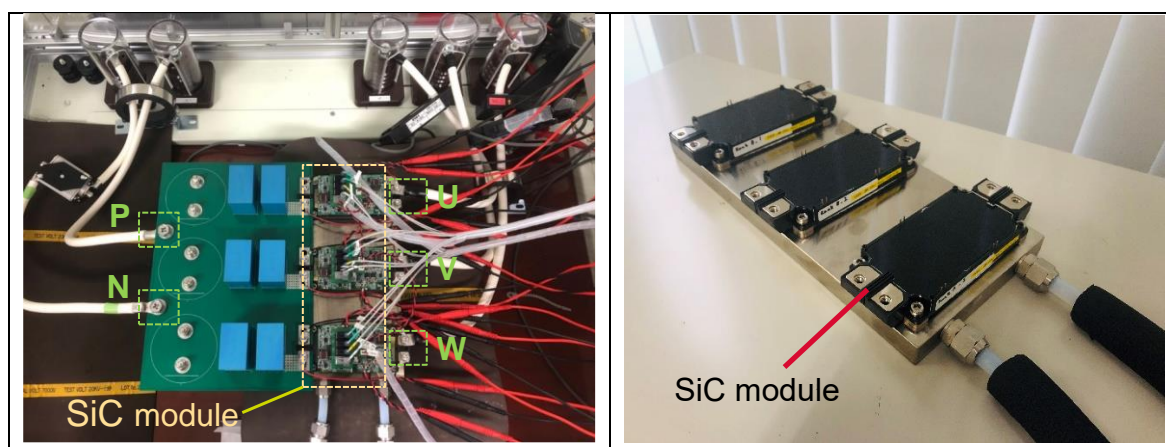


Figure 12. Test Inverter (DUT Inverter)

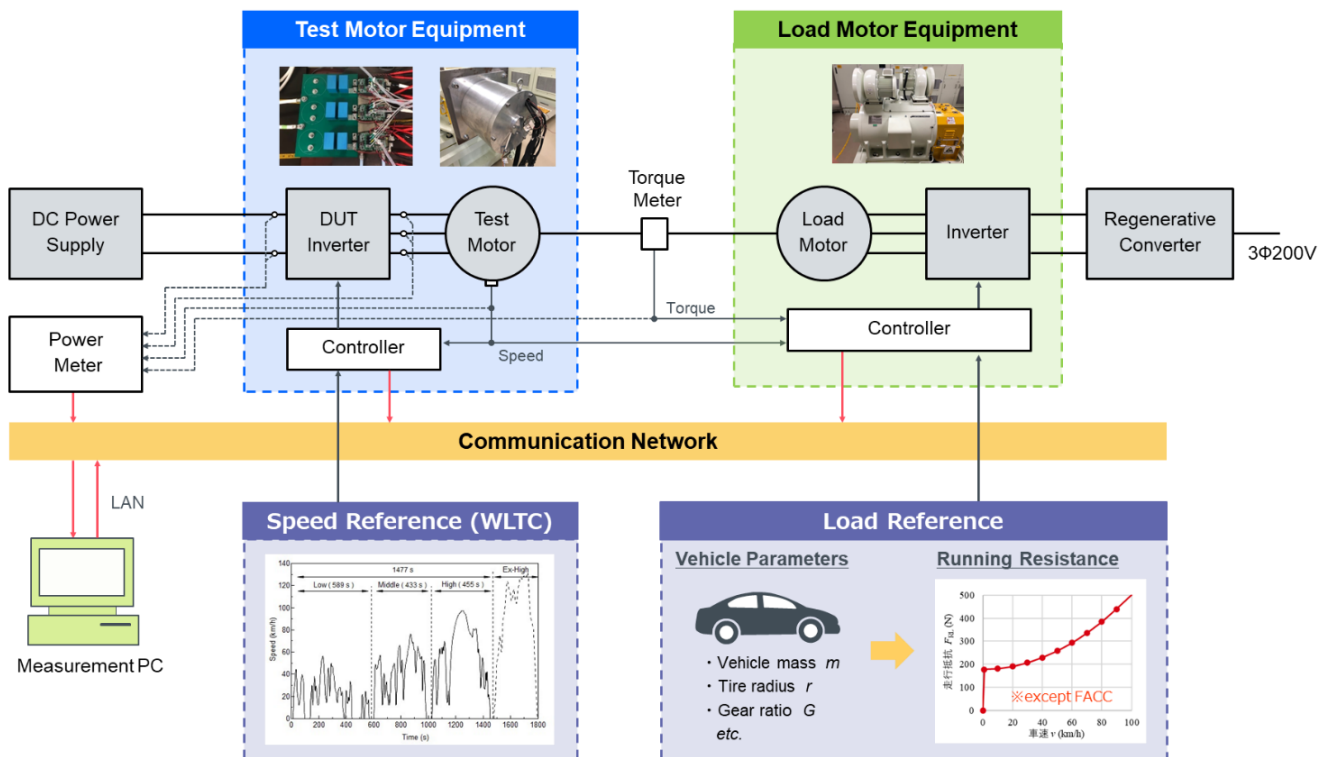


Figure 13. Motor Test Bench / Control System Block Diagram

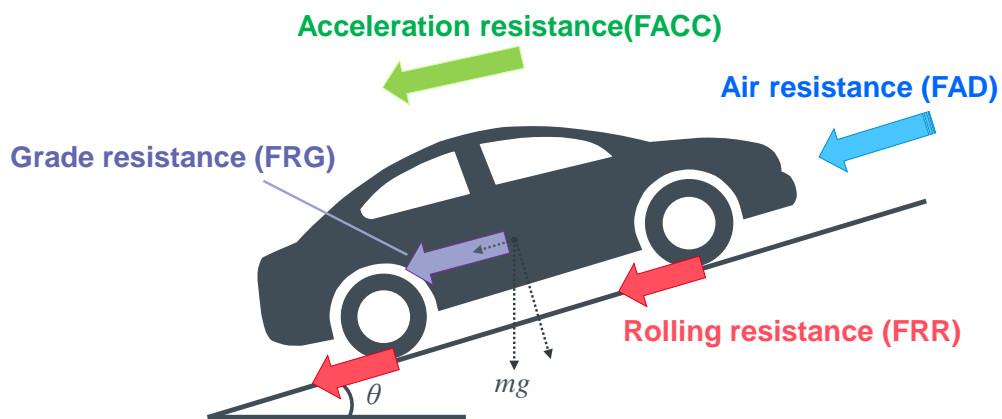


Figure 14. Running Resistance

$$F_{AD} = \frac{1}{2} \cdot C_d \cdot A \cdot \rho \cdot v^2 \quad (15)$$

$$F_{RR} = \mu \cdot m \cdot g \cdot \cos\theta \quad (16)$$

$$F_{RG} = m \cdot g \cdot \sin\theta \quad (17)$$

$$F_{ACC} = (m + \Delta m) \cdot \alpha \quad (18)$$

Where C_d : coefficient of drag, A : frontal projected area, ρ : dry air density, v : vehicle speed, μ : rolling resistance coefficient, m : vehicle weight, Δm : equivalent inertial mass of rotating body, α : acceleration, g : gravitational acceleration, θ : angle between vehicle and road surface.

[3] International Standard WLTC Mode Fuel Efficiency Test for Simulated Driving

The Worldwide Harmonized Light Duty Driving Test Cycle (WLTC) shown in Figure 15 is a driving cycle specified in the Worldwide Harmonized Light Vehicles Test Procedure (WLTP), which was adopted as the Global Technical Regulation (GTR) at the 162nd World Forum on Harmonization of Vehicle Standards (WP29) held at the United Nations Economic Commission for Europe in 2014. This cycle consists of Low, Middle, High, and Extra-High speed phases. In Japan, test vehicles are driven in the driving cycle except for the Extra-High phase to measure exhaust emissions and fuel consumption.

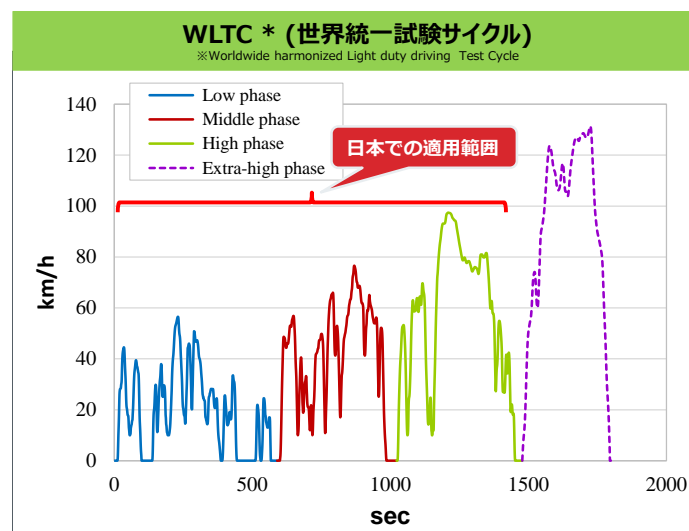
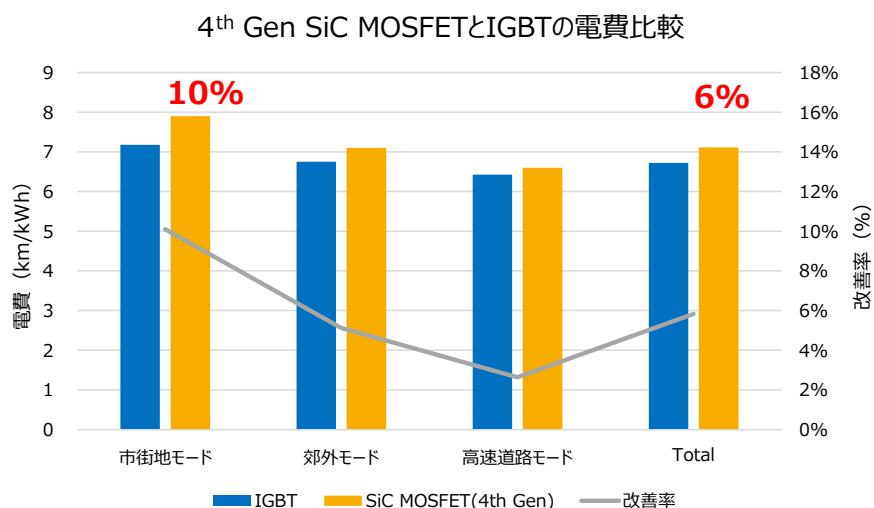


Figure 15. Overview of WLTC (Worldwide harmonized Light duty driving Test Cycle)

Using the aforementioned motor test bench, ROHM conducted a driving cost test using 4th generation SiC MOSFETs and IGBTs in the inverter by inputting the conditions of a simulated WLTC driving cycle.

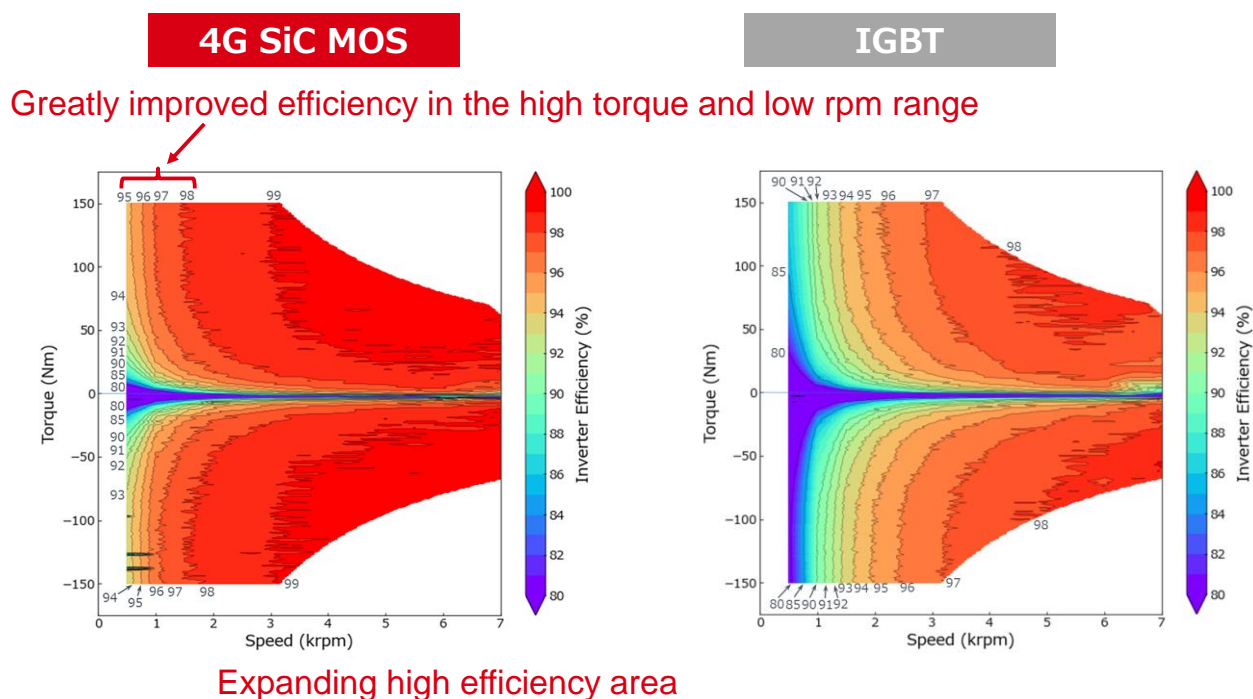
Figure 16 shows the results of the cost test assuming a C-segment class EV, demonstrating that replacing the conventional IGBTs with 4th generation SiC-MOSFETs can improve the cost in all speed phases of the WLTC driving cycle. The total power cost was improved by about 6% compared to the IGBTs, and by about 10% in the urban mode.

For reference, Figure 17 shows a graph of the inverter efficiency map (based on the NT curve, with information on efficiency added). From this result, we can see that the efficiency in the high torque and low RPM range, which is frequently seen in urban driving, has been greatly improved.



Total electricity cost improved by 6%,
The cost in urban mode by 10% improvement compared to IGBT,

Figure 16. Electricity Cost Test Result



(Driving pattern: WLTC Class 3b, assumed vehicle: C segment, motor: permanent magnet synchronous motor 100kW / 800V)

Figure 17. Inverter Efficiency Map in WLTC Electric Cost Test

This section shows how a 6%-10% improvement in performance in the electric cost test can lead to user benefits.

It will be easier to understand if we think in terms of running cost (electricity bill) per mile traveled and reduction of onboard battery capacity. As shown in Table 3, a 5.5% improvement in electricity costs compared to IGBTs results in a reduction of 2,000 yen for a distance of 10,000 km, or 55,000 yen for a car equipped with a 100 kWh battery (Figure 18).

Table 3 Improved Electricity Costs and User Benefits

Device used	Electricity costs	Electricity bill per 1km	At 10,000 km	With a 100kWh battery
ROHM SiC (4 th Gen)	7.11km/kWh	3.52 yen/km (3.20 cent US)	35,200 yen (320.00US\$)	945,000 yen (8590.91US\$)
IGBT	6.72km/kWh	3.72 yen/km (3.38 cent US)	37,200 yen (338.18US\$)	1 million yen (9090.91US\$)

(Calculated assuming that the electricity bill is 25 yen / kWh. and the battery is 1 million yen / 100kWh, applied currency conversion rate of 110 yen/US\$)

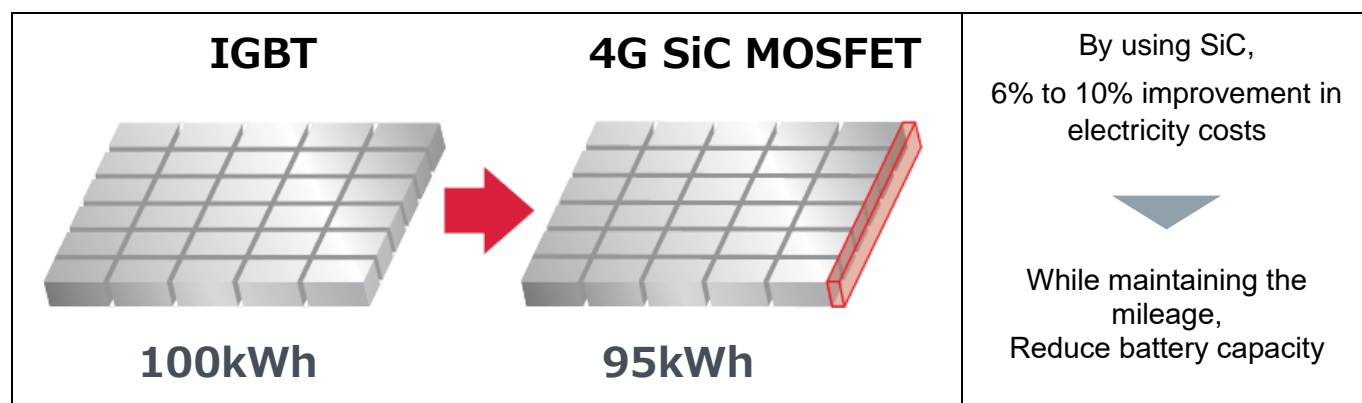


Figure 18. Battery Reduction Effect

3.2 Evaluation of Totem-pole PFC

Totem-pole PFC is a topology that has attracted a great of attention in recent years as a PFC converter that can target high efficiency. In addition, V2G is being considered worldwide to stabilize the microgrid system and contribute to balancing supply and demand, and bidirectional operation has become important.

Figure 19 shows the circuit block diagram. The left leg (S1, S2) is for high frequency switching, and the right leg (S3, S4) is for commercial frequency (low frequency) rectification.

Figure 20 shows the operation diagram by state. During the positive half cycle of the commercial AC, the totem pole low side FET (S2) performs high frequency switching as a boost converter (Figure (a): period D). SiC MOSFETs have a very fast recovery time, and the effect of this power loss is small, so they are a good match for Totem-pole PFC power devices. Next, during the negative half cycle of the commercial AC, the totem-pole high-side FET (S1) acts as a boost converter, switching at high frequency (Figure (c): period D), while S2 acts as a rectifier (Figure (d): periods 1-D). S3 and S4 switch every half cycle of the commercial AC.

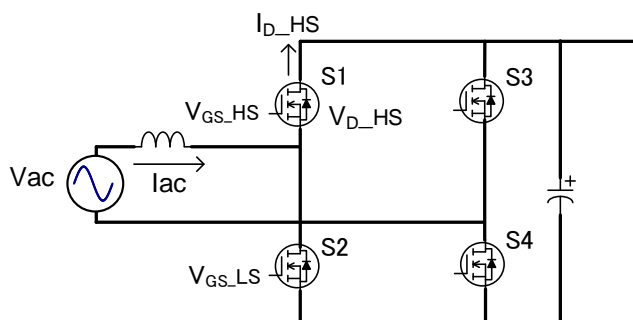


Figure 19. Totem-pole PFC Block diagram

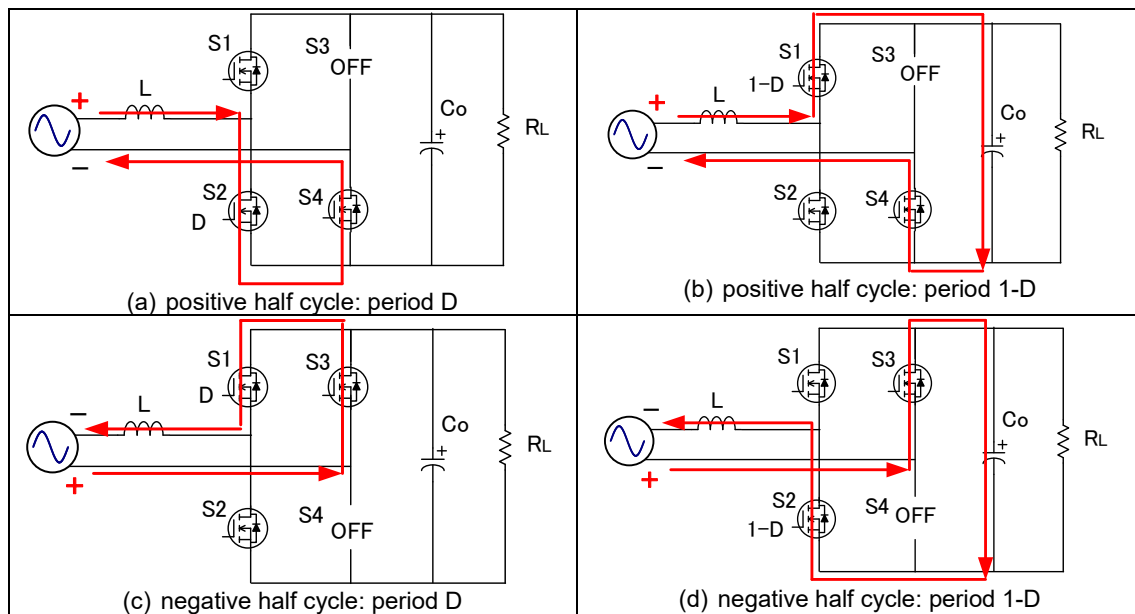


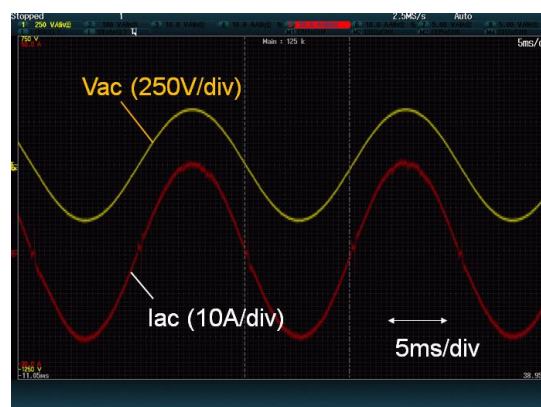
Figure 20. Operation Diagram by State

In order to verify the contribution of the 4th Generation SiC MOSFETs to the loss reduction of the Totem-pole PFC, an experiment was conducted using the actual board. Table 4 shows the evaluation conditions of the PFC and the specifications of the SiC devices used. When the output voltage is 400V, a SiC MOSFET with 750V breakdown voltage is matched. In this case, SCT4045DR is used.

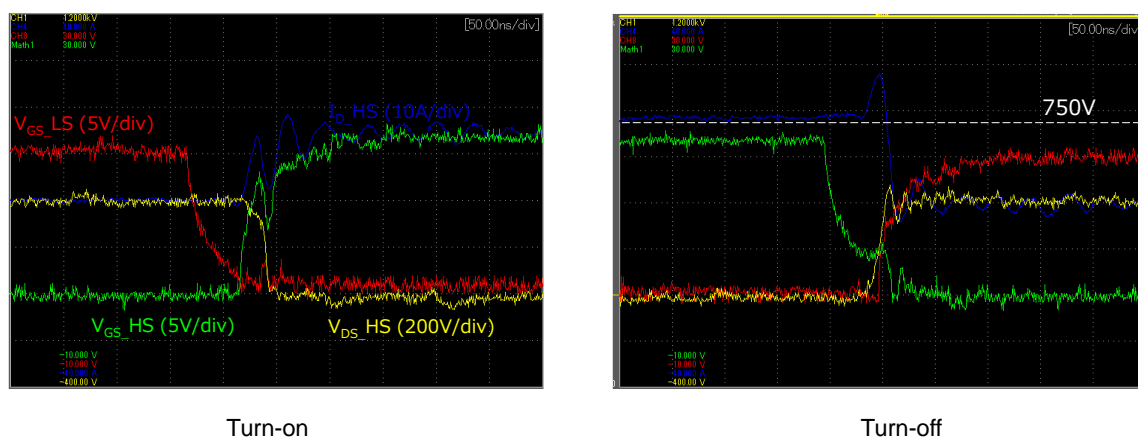
Figure 21 shows the switching waveforms on the board, showing very short turn-on and turn-off times of 20ns-30ns. Figure 22 shows the measured efficiency, which is over 98% at 1.5kW half load and 97.6% at 3kW full load.

Table 4. PFC Evaluation Condition

Input Voltage	230VAC
Output Voltage	400VDC
Output Power	3kW
Inductance L	500μH
Switching Frequency	65kHz
4 th Gen SiC MOSFET	SCT4045DR 750V/45 mΩ
3 rd Gen SiC MOSFET (as reference)	SCT3060AR 650V/60 mΩ



(a) Vac, Iac waveform (1 cycle)



(b) Waveform at Turn-on, Turn-off

Figure 21. Switching Waveforms

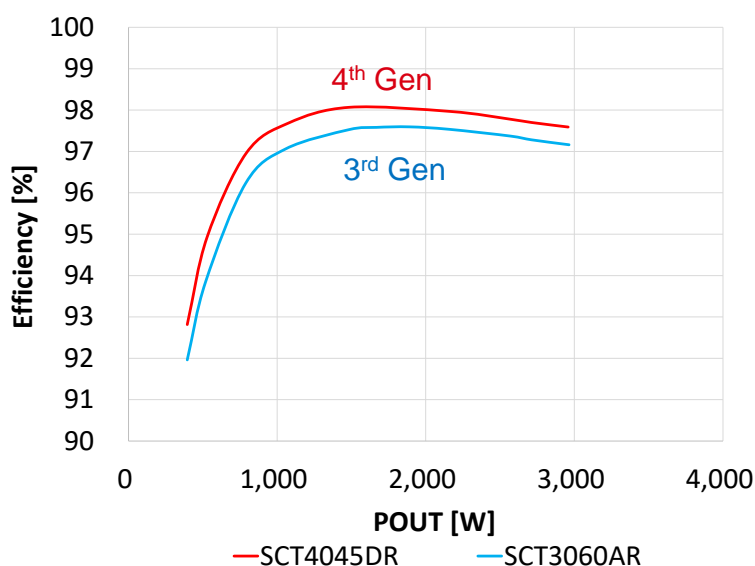


Figure 22. Measured Efficiency




4 Summary

SiC power semiconductors are key power devices for increasing the convenience and power conversion efficiency in applications where high voltage and high current density are progressing, such as EVs, data centers, base stations and smart grids. In the 4th Generation SiC MOSFET, the trade-off of the trench structure has been greatly improved, and the normalized on-resistance has been further reduced. The high-speed switching performance and low on-resistance of the 4th Generation SiC MOSFETs will greatly contribute to the improvement of power conversion efficiency.

In this application note, a 1200V/36m Ω SiC discrete is used for step-down DC-DC converter with 500V input and 7kW output, a 1200V/400A SiC power module is used for EV motor traction inverter with 800V input and 100kW, and a 750V/45m Ω SiC discrete is used for Totem-pole PFC are presented. The usefulness of this technology was demonstrated by evaluating the actual boards. It is expected to contribute to the improvement of power conversion efficiency in many applications in the world.

Finally, the 750 V and 1200 V 4th Generation SiC MOSFET lineups to be released this time are introduced below.

Table 5. 4th Generation SiC MOSFET Product Lineup Table

Product name	V _{DSS} (V)	On-Resistance Typ.(mΩ)	Package
<u>SCT4045DE</u>	750	45	 TO-247N
<u>SCT4026DE</u>		26	
<u>SCT4013DE</u>		13	
<u>SCT4062KE</u>	1200	62	
<u>SCT4036KE</u>		36	
<u>SCT4018KE</u>		18	
<u>SCT4045DR</u>	750	45	 TO-247-4L
<u>SCT4026DR</u>		26	
<u>SCT4013DR</u>		13	
<u>SCT4062KR</u>	1200	62	
<u>SCT4036KR</u>		36	
<u>SCT4018KR</u>		18	
<u>SCT4045DW7</u>	750	45	 TO-263-7L
<u>SCT4026DW7</u>		26	
<u>SCT4013DW7</u>		13	
<u>SCT4062KW7</u>	1200	62	
<u>SCT4036KW7</u>		36	
<u>SCT4018KW7</u>		18	

Product page for 4th Generation SiC MOSFETs: <https://www.rohm.com/products/sic-power-devices/sic-mosfet>

Application information for xEV : <https://www.rohm.com/solution/automotive/xev>

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