Application Note 5SYA 2102-00

Surge currents for phase control thyristors

A number of fault events, both internal in the converter as well as external, will lead to a surge current going through the thyristor. The specific waveform and duration of this current depends on the type of fault and can vary from fractions of milliseconds up to 100 milliseconds or even more. The peak currents are far beyond the nominal rated currents.
During the fault occasions the peak junction temperature can by far exceed the maximum allowed temperature. This may lead to a certain degradation of the thyristor at each surge event. Therefore it is mandatory to know the number of fault cases during the thyristor lifetime to correctly specify the maximum allowed surge current.

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1 Surge currents for phase control thyristors

1.1 Surge current properties

A surge current can appear in various waveforms. Standard tests and datasheet ratings typically use a half-sine wave with duration 10 ms. The following parameters influence the peak junction temperature:

- Initial thyristor junction temperature T_{vj}
- Pulse duration t_p and surge current amplitude I_{TSM}
- Thyristor forward voltage V_T (as a function of temperature and current)
- Thermal impedance Z_{th} of the thyristor
- Mounting force F_M

The losses generated in the thyristor during the surge current event depend on the forward voltage of the device, which again depends on the current and the device temperature. However the voltage can not always be measured or simulated, therefore the surge current integral I^2t is introduced, which eliminates the need to know the forward voltage waveform as long as the current waveform is similar to the specified half-sine pulse.
The surge current integral I^2t of a half-sine wave with current amplitude I_{TSM} is calculated using equation 1 from the Standard IEC 60747 [1]:

$$\int_0^{tp} I^2(t)\cdot dt = \frac{1}{2}\cdot {I_{TSM}}^2 \cdot t_p \qquad \text{Eq.1}$$

The accumulated energy deposited during the pulse can be calculated using equation 2 if v_T, the voltage across the thyristor, and i_T, the current through the thyristor, are measured:

$$E_{surge}(t) = \int_0^t i_T(t)\cdot v_T(t)\cdot dt \qquad \text{Eq.2}$$

The surge current capability is limited by thermal effects. The temperature reached during the surge current event can be calculated through convolution using the power generated in the thyristor and the thermal impedance Z_{th} of the thyristor; this is shown in equation 3.

$$T_{vj}(t) = T_{start} + \int_0^t i_T(\tau)\cdot v_T(\tau)\cdot \dot{Z}_{th}(t-\tau)\cdot d\tau \qquad \text{Eq.3}$$

with

$$\dot{Z}_{th}(t) = \frac{d}{dt} Z_{th}(t)$$

If the voltage cannot be measured or a current different than a half-sine waveform should be simulated, the use of a temperature dependent forward voltage model of the thyristor is appropriate. It is important to properly model the areas of interest, especially the high current and high temperature behaviour of the thyristor.
As the models for forward voltage and thermal impedance normally assume homogeneous conditions, a margin has to be taken into account for non-ideal cases.

1.2 Failure mechanisms

Slightly simplified are three mechanisms responsible for the failure of the thyristor during a current surge. Two of them are connected to the absolute temperature and one to the temperature difference between starting, maximum and end temperature.

a) The thermal stress introduced by these temperature swings will potentially cause damage due to thermal fatigue cumulated during the lifetime of the thyristor. The degradation of the thyristor can lead to changes in the electrical parameters as an increase of the forward voltage or a degradation of blocking capability leading to an increase of the leakage current.

b) If the temperature is too high during the surge current event, a destruction of the device will be caused. The damages to the silicon wafer are so large that the device is not an operational thyristor anymore.

c) Already at a lower temperature the device performance may start changing. At a certain temperature the measures taken to control the carrier lifetime in the device are getting affected. This shows itself as a drift on the trade-off curve between on-state voltage and reverse recovery charge where the device gradually gets a lower on-state voltage and an increased reverse recovery charge.

2 Surge current capability of ABB phase control thyristors

2.1 Definition of surge current capability

The surge current value given in the data sheet is based on the destruction limit of the device. Figure 1 shows a typical waveform during surge current testing. A number of samples are tested with single current pulses with a gradually increased current until they have reached destruction (failure mechanism b). Since only a limited amount of samples can be tested standard statistical methods are applied on the last pass currents in order to determine the specified maximum values. The data sheet values are given at the test conditions with half-sine wave currents with duration 10 ms. The tests are done at the minimum rated mounting force for the devices to ensure that the I_{TSM} value is valid within the range given in the data sheet. During the device lifetime the specified surge currents can only be applied for a few times.

In addition to the surge current value based on the destruction limit ($I_{TSM,datasheet}$) used in the data sheets, a second surge current limit ($I_{TSM,electrical\_change}$) is given in table 1. Up to this surge current there will be no drift on the trade-off curve and the on-state voltage and reverse recovery current will remain stable (not being affected by failure mechanism c).
Howewer if too many pulses of this amplitude are applied there could though be damages to the device due to thermal fatigue (failure mechanism a).

In the phase control thyristor data sheet revisions that began in 2013 the figures with surge current for one half-sine pulse as function of pulse width and surge current for multiple 10 ms half-sine pulses have been removed. Since many fault cases have a different wave shape than half-sine, for instance the asymmetric fault current from a synchronuous machine or the discharge current in a crowbar, these curves are of little practical use and since they also can be misleading it was decided to take them out of the data sheet.

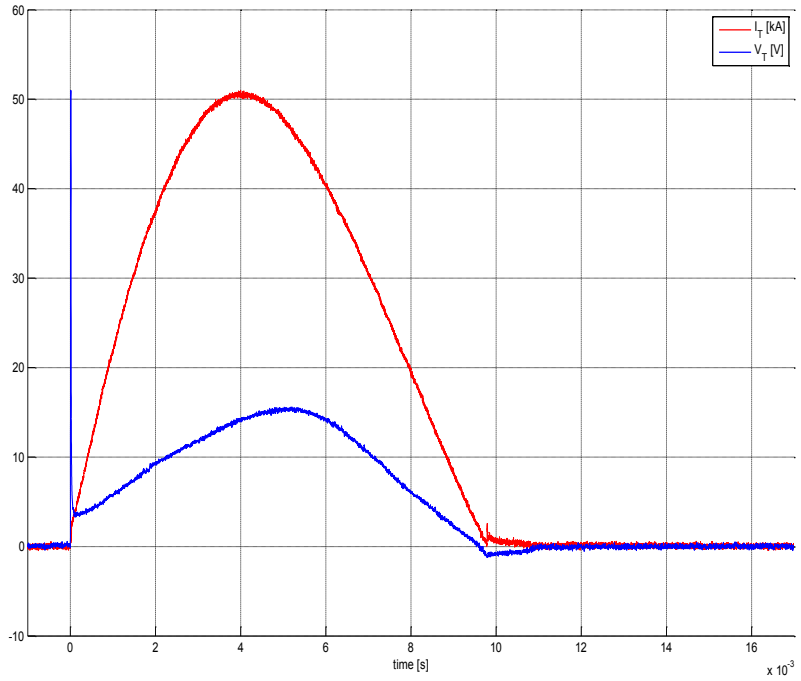

Figure 1 Typical wave forms at surge current testing for a 5STP 25L5200

PCT type	$I_{TSM,datasheet}$ without reapplied voltage [kA]	$I_{TSM,electrical\_change}$ [kA]
5STP 07D1800	9.0	7.7
5STP 42L1800	64.0	62.0
5STP 50Q1800	94.0	79.9
5STP 06D2800	8.8	8.4
5STP 33L2800	65.5	62.7
5STP 45N2800	77.0	65.8
5STP 45Q2800	77.0	65.8
5STP 04D4200	7.1	6.9
5STP 12F4200	17.3	12.8
5STP 28L4200	54.0	46.2
5STP 38N4200	64.5	59.7
5STP 38Q4200	64.5	59.7
5STP 04D5200	6.1	5.7
5STP 17H5200	34.0	25.4
5STP 25L5200	50.5	47.0
5STP 25M5200	50.5	47.0
5STP 34N5200	63.0	55.9
5STP 34Q5200	63.0	55.9
5STP 52U5200	99.0	84.3
5STP 03D6500	4.7	4.6
5STP 03X6500	4.7	4.6
5STP 08F6500	15.1	11.5
5STP 08G6500	15.1	11.5
5STP 12K6500	31.5	22.2
5STP 18M6500	47.5	40.7
5STP 26N6500	65.0	42.4
5STP 42U6500	86.0	73.4
5STP 20N8500	47.5	42.7
5STP 20Q8500	47.5	42.7

Table 1 Surge current ratings ($I_{TSM,datasheet}$) without reapplied voltage (t_p = 10 ms, T_{vj} = 125 °C, sine half wave, $V_D = V_R$ = 0 V after surge)

2.2 Reapplied reverse voltage

The surge current limits described so far will not allow any voltage to be reapplied directly after the pulse, because the thyristors are running too hot during the pulse and will not be able to stabilize the leakage current. If reapplied voltage is needed, a derating has to be taken into account to prevent thermal runaway after the pulse. Table 2 shows the values for a number of ABB thyristors for the case with a 10 ms half-sine current followed by a reverse voltage with an amplitude of 60 % of the rated repetitive reverse voltage for the device.

PCT type	$I_{TSM,datasheet}$ with reapplied reverse voltage [kA]
5STP 07D1800	7.1
5STP 42L1800	40.0
5STP 50Q1800	88.0
5STP 06D2800	6.9
5STP 33L2800	49.5
5STP 45N2800	60.0
5STP 45Q2800	60.0
5STP 04D4200	5.9
5STP 12F4200	12.0
5STP 28L4200	42.5
5STP 38N4200	51.0
5STP 38Q4200	51.0
5STP 04D5200	4.8
5STP 17H5200	24.5
5STP 25L5200	37.0
5STP 25M5200	37.0
5STP 34N5200	45.5
5STP 34Q5200	45.5
5STP 52U5200	78.0
5STP 03D6500	3.6
5STP 03X6500	3.6
5STP 08F6500	9.7
5STP 08G6500	9.7
5STP 12K6500	19.4

PCT type	$I_{TSM,datasheet}$ with reapplied reverse voltage [kA]
5STP 18M6500	29.5
5STP 26N6500	40.0
5STP 42U6500	64.0
5STP 20N8500	31.5
5STP 20Q8500	31.5

Table 2 Surge current ($I_{TSM,datasheet}$) with reapplied reverse voltage (t_p = 10 ms, T_{vj} = 125 °C, sine half wave, $V_R = 0.6*V_{RRM}$ after surge)

2.3 Reapplied forward voltage

In fuseless systems it is often a requirement that the thyristor can block forward voltage reapplied after the surge current. The device capability is not included in the data sheets since there are too many factors included to make an appropriate graph. Application specific support can be provided upon request.

3 References

1. IEC Standard 60747 “Semiconductor Devices”

4 Revision history

Version	Change	Authors
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