Application Note 5SYA 2093-00

Thermal design and temperature ratings of IGBT modules

A proper thermal design is crucial for a reliable operation of power semiconductors. A violation of the temperature ratings can lead to a reduced safe operating area and consequently a sudden device failure or to a reduced operational lifetime.
IEC 60747-9 gives a range of temperature ratings for IGBTs like storage temperature (T_{stg}), case temperature (T_c) and virtual junction temperature (T_{vj}). The ratings are though not described in detail. Knowing the thermal resistance/impedance of the device and the dissipated losses the junction temperatures can be calculated [2].
The aim of this application note is to describe the temperature ratings and shed some light to the topics like thermal resistance and equivalent thermal circuits.

Contents

		Page
1	Temperatures	3
1.1	Junction temperature	3
1.2	Operating junction temperature $T_{vj(op)}$	3
1.3	Case temperature T_c	3
1.4	Heatsink temperature T_h	3
1.5	Storage temperature T_{stg}	3
2	Thermal impedance	3
2.1	Definition and test method	3
2.1.1	Measurement of the junction temperature	3
2.1.2	Zth Test procedure	
3	Termal equivalent network	5
3.1	Cauer Model	5
3.2	Foster Model	6
3.3	Connecting Module and Heatsink	6
3.3.1	Series connection of Foster Models	6
3.3.2	Series connection of Cauer Models	6
3.4	Thermal Interface Resistance	7
4	Conclusions	7
5	References	8

1 Temperatures

1.1 Junction temperature

The junction temperature describes the temperature inside the chip which is relevant for the losses and safe operating area. Since the chip temperature is not homogenous the term virtual junction temperature is used (T_{vj}). The virtual junction temperature is an average chip temperature assuming homogenous cooling of the device. Also the thermal impedance/resistance ($Z_{th(j-c)}$) / $R_{th(j-c)}$) is defined with the virtual junction temperature (IEC 60747-9, 6.3.13).

$T_{vj,\ max}$ describes the maximum allowed dynamic junction temperature in the device on-state. Even under dynamic overload the device is not allowed to exceed the $T_{vj,\ max}$ value in on-state. Prior a switching event or in off-state with applied voltage the junction temperature of the device needs to be within the specified range of operating junction temperature $T_{vj(op)}$.

1.2 Operating junction temperature $T_{vj(op)}$

The operating junction temperature is relevant for the device operation and must be considered as the practical design value. The device must be operated within the $T_{vj(op)}$ range. When calculating the junction temperature for normal switching using the conduction losses, switching losses and the thermal impedance, the junction temperature has to stay always between the minimum and maximum specified value of $T_{vj(op)}$ even in case of overload situations. In practice prior the last switching event the junction temperature must stay below $T_{vj(op)}$, max. The transient temperature rise due to the switching losses in the switching event can be ignored, provided the device is operated within its safe operating area and T_{vj} does not exceed $T_{vj,\ max}$.

1.3 Case temperature T_c

The case temperature (T_c) defines the allowed temperature range of the module case in operation. The case temperature range can differ from virtual junction temperature range. For instance the maximum case temperature can be lower than $T_{vj(op),max}$. This is because the plastic materials used for power modules cases have temperature limits. This though usually does not restrict operation in application conditions since there is always a temperature gradient from junction to case and devices operated with T_{vj} = 150 °C usually have a case temperature of less than 125 °C.

In order to test electrical device parameters in single pulse mode at higher junction temperatures it is possible to passively heat devices up to $T_c = T_{vj(op),max}$. But the device housing materials might be degraded if $T_{vj(op),max} > T_{c,max}$, in this case the modules should not be used for field operation afterwards.

When testing electrical device parameters at elevated case temperatures with passive heating thermal run-away must be avoided [3].

1.4 Heatsink temperature T_h

The heatsink temperature describes the surface temperature of the heatsink/cooler on which the power-module is mounted. In some cases (e.g. base-less modules) the thermal impedance of the module is defined with the heatsink temperature ($R_{th(j-h)}$ / $Z_{th(j-h)}$).

1.5 Storage temperature T_{stg}

The storage temperature describes the temperature range in which devices are allowed to be stored. Cold temperature storage at -40 or -55 °C is verified with a storage test. The maximum temperature gradient when heating up from cold temperature is limited to 1 K/min (averaged over a maximum time of 5 minutes) [4].

2 Thermal impedance

2.1 Definition and test method

The thermal impedance (Z_{th}) and thermal resistance (R_{th}) are measured according to IEC 60747-9 6.3.13.

2.1.1 Measurement of the junction temperature

The junction temperature is indirectly measured with a temperature sensitive device characteristic such as V_{CEsat}, V_F at low current (to prevent heating effects from the measurement) or the threshold voltage $V_{GE(TO)}$.

For this reason a calibration curve of eg. $V_{CEsat} = f(T_j)$ has to be recorded prior the R_{th}/Z_{th} measurement.

The calibration curve is recorded with homogenuous external heating of the power module. It is crucial that a thermal equilibrium is reached at each measurement point. This kind of indirect T_j measurement offers an averaged junction temperature.

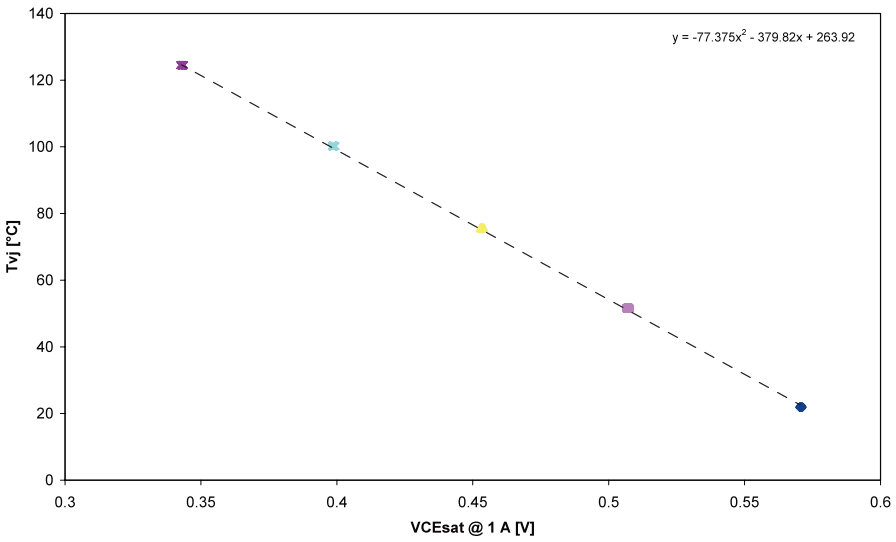

Figure 1: Calibration Curve $V_{CEsat} = f(T_{vj})$

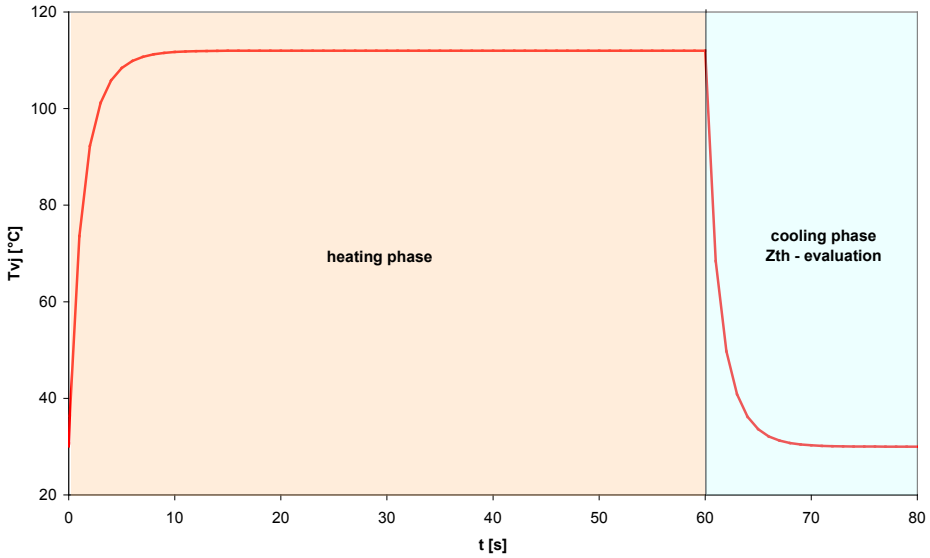

Figure 2 Temperature profile during Z_{th} Measurement

2.1.2 Z_{th} Test procedure

In order to measure the thermal impedance junction to case the measured power modules are mounted onto a water cooler according to the latest mounting recommendations [6].
Now the module is heated in on-state with constant power until all temperatures are stable (fig. 2). Then the current is switched off by means of an external switch. The thermal impedance is measured during the following cool-down period. T_{vj} is measured using the in 2.1.1 described indirect measurement method.
The case temperature is measured with a temperature-probe either in the base-plate close to the surface or as a surface-probe. The location of the case-temperature-probe should be directly below the heated chips. Since the temperature-probes (thermo-couple or PT100/1000) have limited response time transient recordings especially in the lower time regime have to be treated with care and should be verified with FE-simulations. Unfortunately the case temperature is not homogenuous, especially due to interface compound, which has to be considered when evaluating the thermal impedance.
The thermal impedance is calculated based on the measured constant power in the heating phase and the measured temperatures in the cooling phase:

$$Z_{th((j-c)}(t) = \frac{T_j(t) - T_c(t)}{P} \quad (1)$$

Since the cooling phase is used the time scale during the measurement needs to be reversed.

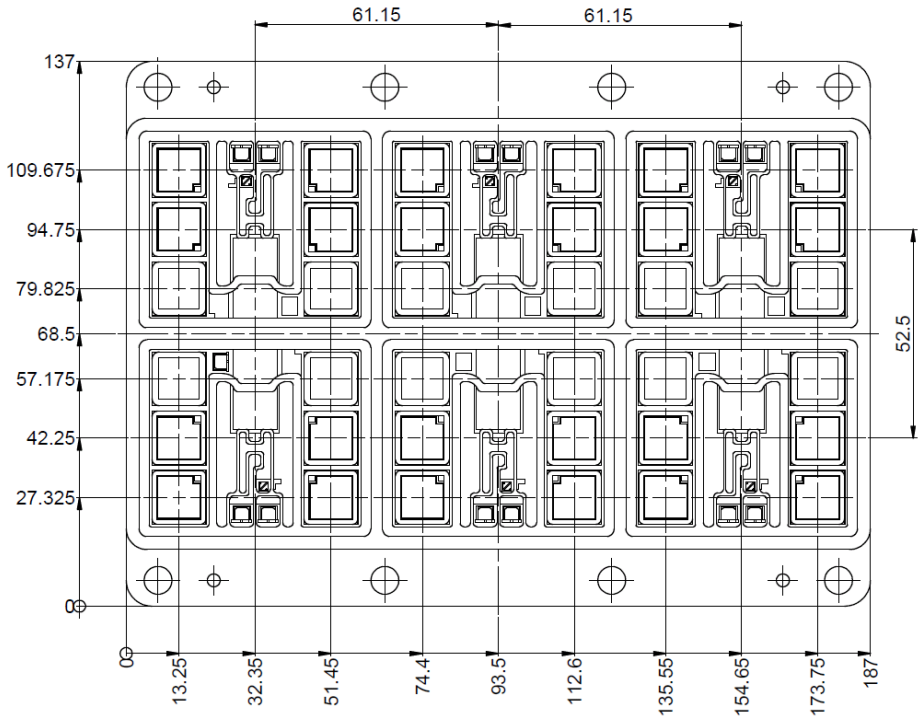

Figure 3: Chip Positons in a HiPak2 type module

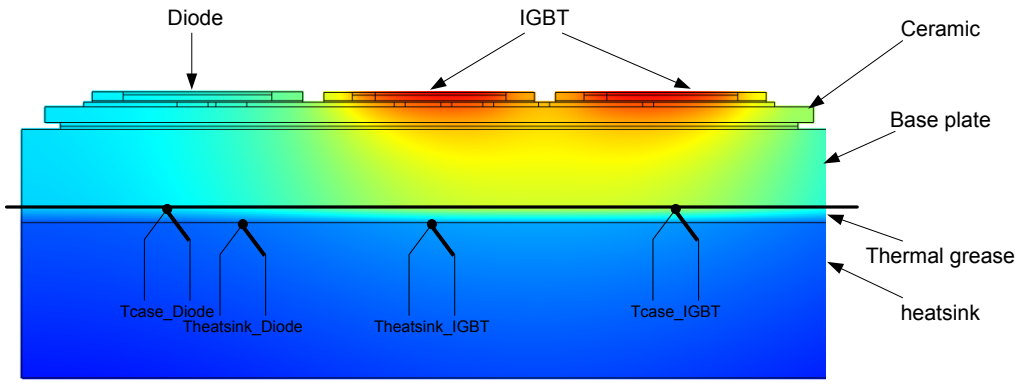

Figure 4: Location of case-temperature-probes

3 Thermal equivalent network

3.1 Cauer Model

With the Cauer Model a realistic physical representation of the transient thermal behaviour is theoretically possible. With the appropriate knowledge of the material properties of the layers and the module construction it is possible to create such a model. Though the assumption of heat-spread is critical and thicker layers might need to be divided into several R/C terms.

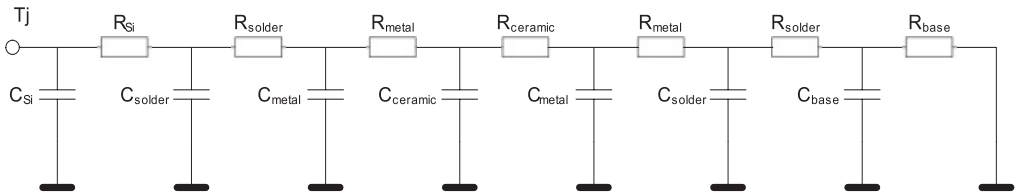

Figure 5: Cauer Model

Figure 6 shows the Zth characteristic for a power module evaluated with different methods in order to show the limitation of a simplified Cauer model. The red curve represents the most realistic case. The FE simulation is set up considering the upper third of the IGBT chip volume as heat source and Tj is considered as the average temperature of the heated IGBT volume (upper third). The dashed light blue curve assumes the whole active area times chip thickness (chip without termination and gate pad) as heat source and Tj is again the average of the heated volume. For both FE simulations the case temperature is evaluated as the average case temperature over the area underneath all chips and the measured case area is equal as the full chip area.

The solid dark blue line represents an evaluation using a Cauer model as depicted in figure 5. The simplified Cauer model shows somewhat too optimistic values below 10 milliseconde (ms). This is because it assumes the full active chip volume as heat source. In the marked time region of 100 ms the Cauer model shows too low values since the base-plate (5 mm thick) is represented by only one R/C term. Thus thicker layers would need to be divided in several R/C terms if more accuracy is needed.

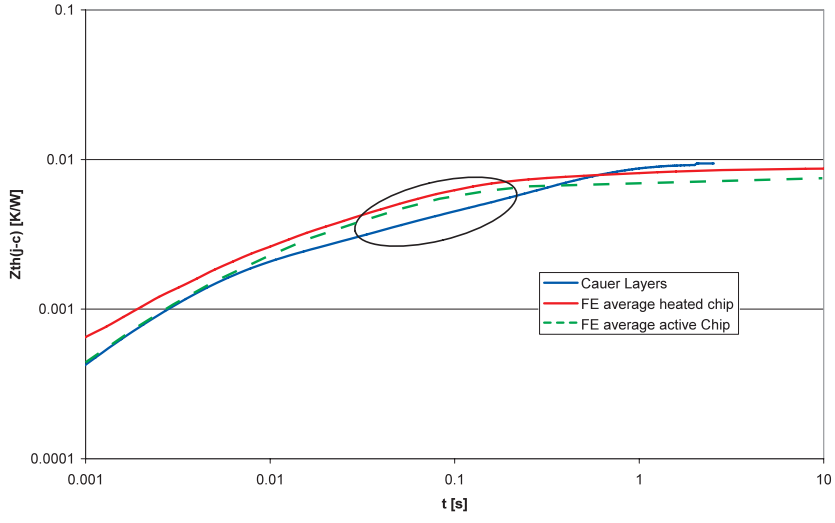

Figure 6 : Zth curve

3.2 Foster Model

The datasheets typically show the Zth characteristics as so called Foster Model. The Foster Model is fitted to the numeric Z_{th} characteristics and has no physical meaning. The amount of RC-terms are irrelevant, the model just needs to fit.

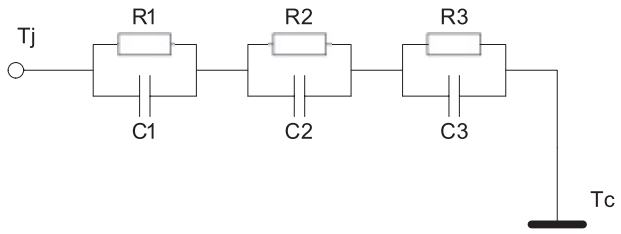

Figure 7: Foster Model

The analytical function of the thermal impedance can be described with the terms R_i and τ_i ($\tau_i = R_i \times C_i$):

$$Z_{th(j-c)}(t) = \sum_{i}^{n} R_i(1 - e^{-t/\tau_i}) \qquad (2)$$

This model is suitable if a constant case temperature can be assumed. Nevertheless this is not necessarily given in the application. Thus the thermal model of the power module needs to be connected with a thermal model for the heatsink including the interface material (e.g. case to ambient).

3.3 Connecting Module and Heatsink

In the real world the power module is mounted on a heatsink using an interface compound such as thermal grease to make an as good as possible thermal contact. This means the thermal impedance of the interface compound and the heatsink are series connected to the thermal impedance of the module.
Connecting thermal models in series is generally critical and needs to be treated with care. The heat spreading and thus the thermal impedance of the power module depend on the cooler efficiency case to ambient. Water cooled heatsinks offer efficient de-heating and the heat spreading is lower. Less efficient air cooled heatsinks cause a larger heat spreading. Therefore the thermal impedance of the power module tends to get lower.
The effect to the $Z_{th(j-c)}$ is though only little and in the range of less than 1 %. The reason can be found in the rather large thermal resistance of the thermal interface material (TIM) that practically shields the heatsink from the module.
The heat spreading angle in the module is thus mainly defined by the R_{th} of thermal interface material. When measuring the module R_{th}/Z_{th} ABB uses efficient water cooled heatsinks in order to resemble the worst case situation for the module Z_{th}.
Additionally the uncertainty and inhomogeneity of the thermal resistance of the interface material is rather high. Even with the highest quality standards for application of the TIM, the thermal resistance of the interface material is in the same magnitude as the module itself but the homogeneity over the full area is much worse. Thus a rather large variation of the local R_{th} and thus as well the case temperature has to be expected.
The most reliable thermal impedance junction to ambient $Z_{th(j-a)}$ can be achieved by a direct measurement of the full setup including the module, TIM and heatsink.

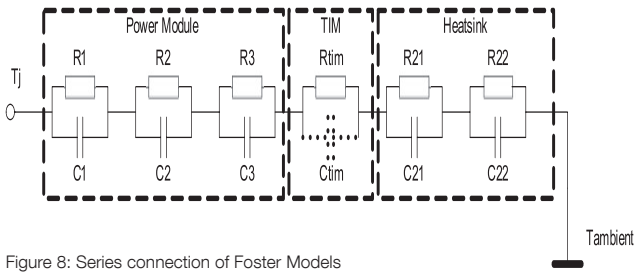

Figure 8: Series connection of Foster Models

3.3.1 Series connection of Foster Models

A straight forward approach is the series connection of the Foster model offered in the module datasheet, the thermal resistance of the thermal interface material TIM ($R_{th(c-h)}$) and the thermal resistance of the heatsink.
The series connection of Foster models yields in inaccurate results especially in the lower time regime. Figure 9 shows the calculated temperature response of a typical configuration HiPak2 module mounted onto a water cooler with thermal grease and a power step of 1 kilowatt (kW).
The dashed lines represent the temperatures calculated using a series connection of Foster models and the solid lines a realistic approach using an appropriate Cauer model.
In case of the Foster model the power flows via the heat capacitors directly to the thermal resistance of the TIM causing an immediate temperature step of the case and thus as well a step response in the junction temperature. This is a significant deviation to the realistic solid lines. As a consequence the case and junction temperatures are too high up to around 4..5 s. After this time period (when the module Zth is close to the steady state) the temperatures are more realistic for both type of models.
Thus especially in case of heatsinks with low time constants (water cooled) the simplification of series connection of Foster models can introduce significant errors.

3.3.2 Series connection of Cauer Models

At first glance the series connection of Cauer models looks not critical since it resembles the physical behaviour where the power reaches the heatsink with delay (when the module heat capacitors are charged). This can be the case if the series connected models are very close to the real physics.
A transformation of the datasheet characteristics (diagram, Foster model) to a Cauer model is possible but not biunique and can

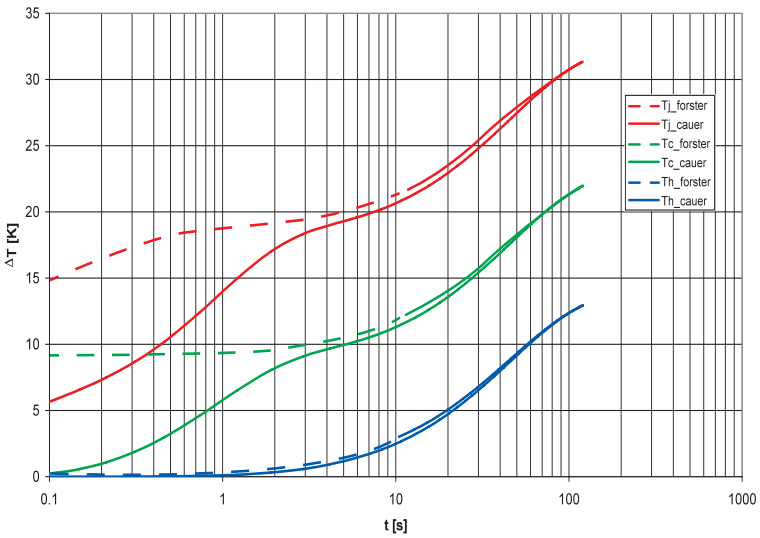

Figure 9: Temperature response of series connected models

lead to different R_{th}/C_{th} terms for the same $Z_{th(j-c)}$ characteristics. Such a transformed model also does not represent the physical layers and especially the total Cth of such a model can deviate by orders of magnitude from the total effective heat capacity of the power module.
Thus if such a model is connected to a heatsink the $Z_{th(j-a)}$ characteristics of the combined model can be significantly wrong.

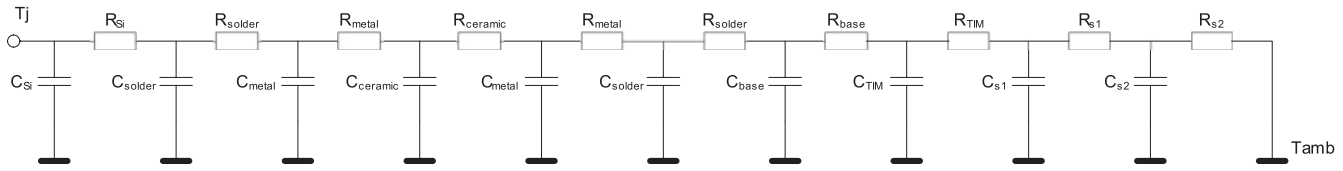

Figure 10: Series connection of Cauer Models

3.4 Thermal Interface Resistance

The module datasheet specifies a typical interface resistance which can be achieved by a proper application of a suitable thermal interface material.
A perfect applied TIM allows metal to metal contact between Module and Heatsink where possible and fills the remaining gaps. This leads inevitable to a large spread of the local thermal interface resistance with order of magnitude differences between the metal-metal contacts and the areas where the TIM needs to fill the gap. Consequently the case temperature is far from being homogenuous.
Undisputable the biggest uncertainty in the whole thermal design thus comes from the TIM layer, first because of the non uniform thermal resistance and secondly also from ageing phenomena.

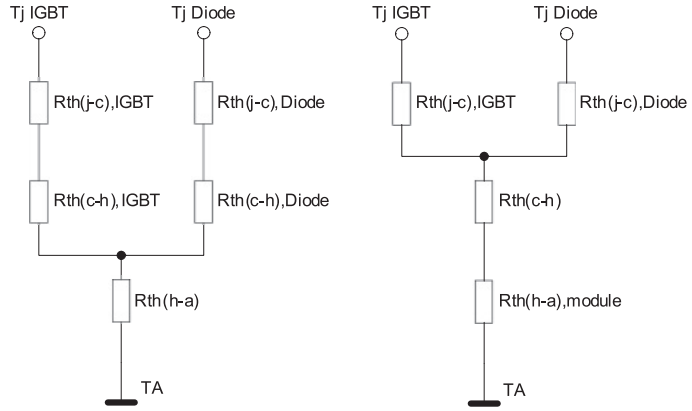

Figure 11: Modelling of the thermal interface

In newer datasheets thermal interface resistance ($R_{th(c-h)}$) is usually stated separately for IGBT and Diode. This is a more realistic simplification if the cross-talk between IGBT and Diode is considered.
Nevertheless if for some reason $R_{th(c-h)}$ for the full module is needed, but the datasheet specifies it separately for IGBT and Diode, a simple parallel connection can be done:

$$R_{th(c-h),module} = \frac{R_{th(c-h),IGBT} \cdot R_{th(c-h),Diode}}{R_{th(c-h),IGBT} + R_{th(c-h),Diode}} \quad (3)$$

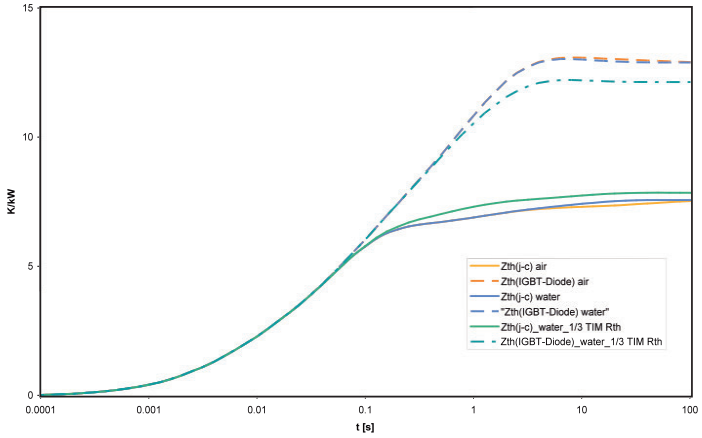

Figure 12: Cross talk IGBT-Diode

Figure 12 shows $Z_{th(j-c)}$ and the cross heating thermal impedance from the IGBT to the Diode in case of a HiPak2 sized module. The difference between air ($R_{th(h-a)}$ = 40 K/kW) and water ($R_{th(h-a)}$ = 10 K/kW) is very little. Though obviously the cross talk Z_{th} ends in a significant higher Rth than $R_{th(j-c)}$, thus the simplified thermal connection between IGBT and Diode is closer to the heatsink than the module case. This also indicates that the thermal heatsink properties do not significantly influence the thermal properties of the module since the heatsink is 'shielded' by the TIM layer.
For experimental reasons the R_{th} of the TIM layer in the simulation was reduced to 1/3 of its original value (6 K/kW). Though this is hardly achievable in reality, it shows that the TIM layer influences the heat-spreading much more than the heatsink. With an efficient TIM layer the heat-spreading in the module will be smaller and thus $R_{th(j-c)}$ increases. Consequently the cross-heating thermal resistance (IGBT-Diode) gets smaller. On the other hand small natural local variations of the TIM layer due to cavities will be to some extend compensated by the heat-spreading in the module. Nevertheless an increase in the $R_{th(c-h)}$ of the TIM will never be compensated by a reduction in $R_{th(j-c)}$ of the module. Thus it will be always worthwhile to have the best possible TIM layer quality.

4 Conclusions

For reliable operation over the expected lifetime of a converter system a proper thermal design is crucial. The uncertainty in connecting different thermal resistance expressions together is rather big and especially the thermal interface material introduces a large vagueness. The most advantageous solution to capture a realistic thermal model is to characterise the full chain of the thermal

resistance from junction to ambient (water/air) with the method proposed in 2.1.2. Later an analytical model (e.g. Foster) can be fitted to this measurement. If the direct measurement is not possible and module and heat-sink models need to be connected, the uncertainty especially for the transient case gets significantly bigger and reasonable margins should be introduced. In this case the most appropriate way with respect to physics is to use series connected Cauer models. Though it is crucial to verify that the Cauer models do match to the module physics (total heat capacity). If for any reasons Foster models are connected together one has to be aware of the limitations of this approach. Transient cases in the range of the module time constant such as the junction temperature ripple due to the AC-output frequency would yield in wrong results. A quick fix can be to calculate short transients only with the thermal impedance of the module and assuming a constant case temperature for these short transient cases.

5 References

[1] IEC Standard 60747 «Semiconductor Devices»
[2] 5SYA2053 «Applying IGBT»
[3] 5SYA2042 «Thermal Runaway»
[4] 5SZK 9111 «Storage of HiPak»
[5] IEC 60068-2-1
[6] 5SYA2039 «Mounting Instructions for HiPak Modules»

The application notes, references [2], [3] and [6] are available at www.abb.com/semiconductors

6 Revision history

Version	Change	Authors
00	Initial Release	Raffael Schnell
		Martin Bayer
		Silvan Geissmann

For more informations:

ABB Switzerland Ltd.
Semiconductors
Fabrikstrasse 3
CH-5600 Lenzburg
Switzerland
Tel: +41 58 586 14 19
Fax: +41 58 586 13 06
E-Mail: abbsem@ch.abb.com
www.abb.com/semiconductors

Application note 5SYA 2093-00 20.08.2013