Application Note 5SYA 2045-01

Thermal runaway during blocking

Since the beginning of semiconductor technology, thermal runaway has been a well-known effect. Thermal runaway occurs when the power dissipation of a device increases rapidly with temperature. A classic example is the thermal runaway during blocking, when the applied voltage causes a leakage current and their product heats up the device. As the device gets hotter, leakage current increases exponentially and so, therefore, does the heating. If the cooling of the device is not adequate, the device will get progressively hotter and will ultimately fail.

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1 Introduction

The recent development of very high-voltage IGBT modules has lead to increased values of dissipated power during off-state, due to their higher blocking voltages, even if the leakage currents remain at similar levels as devices with lower blocking voltage. This can cause problems when such devices are characterised at high temperature (e.g. 125 °C). In this case, the whole measurement system (heating plate, module, chip) is heated up to a constant temperature and no temperature gradient exists to sink the generated heat. This is in strong contrast to real-world applications where the junction temperature may indeed reach a maximum value of 125 °C but the case temperature never exceeds, say, 110 °C allowing leakage current losses to be cooled away across the temperature gradient between junction and case.

This Application Note is intended to describe the limits of thermal stability, which have to be taken into account when testing and operating semiconductor devices. In order to keep the analysis straightforward, a number of simplifying assumptions are made. It should be noted in particular that heating and cooling is generally not homogeneous as assumed here, so a reasonable safety margin is always additionally required. Nevertheless, the findings provide a good guideline for designing cooling requirements.

2 The problem

The power P_{heat} dissipated by the device is simply the applied voltage V_0 times the leakage current I (V_0, T_j) at the said voltage and the respective junction temperature T_j. Usually, a power law can conveniently fit the temperature dependence of the leakage current. Following a well-known rule of thumb, which says that the leakage current doubles every ~11 K, a power law with the base 2 and the characteristic constant T_d = 11 K (temperature increase to double the leakage) is chosen. The current I_0 is then the leakage current at the applied voltage V_0 and the reference temperature T_0:

$$P_{heat} = V_0 \cdot I(V_0, T_j) = V_0 \cdot I_0 \cdot 2^{\frac{T_j - T_0}{\Delta T_d}} \quad (1)$$

The power P_{cool}, which is cooled away from the device, is given by the difference between the junction temperature T_j and the stable reference temperature T_0 (e.g. the controlled cooler or ambient temperature) and the thermal resistance R_{th}:

$$P_{cool} = \frac{T_j - T_0}{R_{th}} \quad (2)$$

NB: Transient effects can be ignored because R_{th} is already the worst case.

In Fig. 1, the generated power (P_{heat}) and the power which is cooled away (P_{cool}) are plotted against the junction temperature. The reference temperature in this example is T_0 = 125 °C. Assuming a 6500 volts (V) HiPak module with a leakage current of 60 milliampere (mA) at 3600 V and 125 °C, the red curve representing P_{heat} is obtained.

The cooled (sunk) power is shown for different thermal resistance values. The blue curve represents a module with sufficient cooling. The black curve shows a module mounted with an inadequate mounting technique and the green curve shows the limit of thermal stability.

Reference to the blue curve of Fig. 1 shows that up to the first

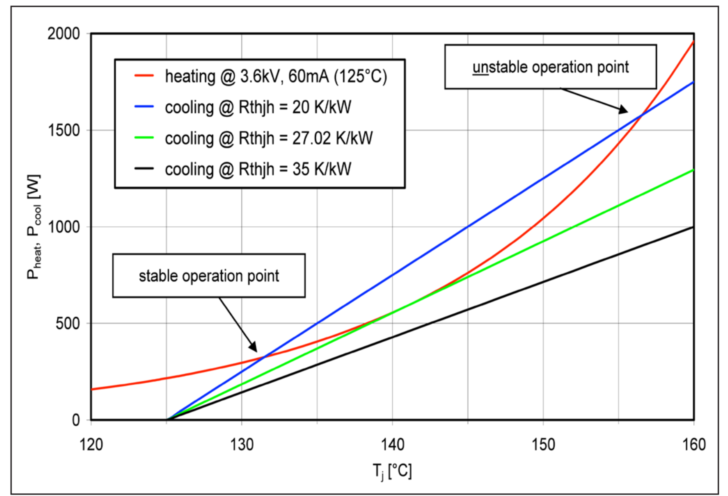

Fig.1: Power balance of a module for different cooling situations. Blue: proper cooling, black: inadequate cooling, green: limit of thermal stability according to E_{qn} (10)

crossing point (stable operating point), the chips will heat up until power balance is reached (e.g. at 131.5 °C). Above this point the junction temperature drops back to the stable operation point. However, if the junction temperature exceeds 156.6 °C (unstable point of operation) the balance of the power is disturbed and the device will continue to heat itself up until it fails.

The black curve shows the power cooled away in case of an inadequate mounting technique (e.g. module not bolted to heat-sink). In this case, P_{heat} is always higher than P_{cool} which means that no stable operating point can be reached and thermal runaway will result.

The necessary cooling power to just reach the limit of thermal stability is shown by the green curve. In this case, the stable point and the unstable point of operation are merged when P_{heat} and P_{cool} are tangential. In such a case, a small thermal imbalance could provoke thermal runaway.

3 Calculating the stability criterion

As already discussed, the limit of thermal stability is the point at which the P_{heat} and P_{cool} curves are tangential. At this point, the heating power P_{heat} and the cooling power P_{cool} have to be equal and the derivatives (with respect to the junction temperature) of both curves must also be equal:

$$P_{heat} = P_{cool} \quad \wedge \quad \frac{dP_{heat}}{dT_j} = \frac{dP_{cool}}{dT_j} \quad (3)$$

The derivative of the heating function is given in E^{qn} (4). Note that the derivative is given by the original function times a constant.

$$\frac{dP_{heat}}{dT_j} = V_0 \cdot I_0 \cdot 2^{\frac{T_j - T_0}{T_d}} \cdot \frac{\ln 2}{\Delta T_d} = P_{heat} \cdot \frac{\ln 2}{\Delta T_d} \quad (4)$$

The derivative of the cooling function is simply the reciprocal of the thermal resistance:

$$\frac{dP_{cool}}{dT_J} = \frac{1}{R_{th}} \quad (5)$$

Starting with the right-hand side of E^{qn} (3), one obtains a formula for P_{heat} that depends on T_d and R_{th} only. Putting this result into the left-hand side of E_{qn}. (3), one determines the critical temperature at which the two curves are tangential.

$$\frac{dP_{heat}}{dT_j} = \frac{dP_{cool}}{dT_j} \Rightarrow P_{heat} \cdot \frac{\ln 2}{\Delta T_d} = \frac{1}{R_{th}} \Leftrightarrow P_{heat} = \frac{\Delta T_d}{R_{th} \cdot \ln 2} \quad (6)$$

$$P_{heat} = P_{cool} \Rightarrow \frac{\Delta T_d}{R_{th} \cdot \ln 2} = \frac{T_{j,crit} - T_0}{R_{th}} \Leftrightarrow \underline{\underline{T_{j,crit} - T_0 = \frac{\Delta T_d}{\ln 2}}} \quad (7)$$

Interestingly, the difference between the critical junction temperature $T_{j,crit}$ and the constant reference temperature R_0 is independent of the applied voltage V_0, the leakage current I_0, and the thermal resistance R_{th}! The only influencing factors are the parameters (T_d and 2) describing the temperature dependence of the leakage current.
Using this result the corresponding leakage current at $T_{j,crit}$ can be calculated:

$$I_{crit} = I(V_0, T_{j,crit}) = I_0 \cdot 2^{\left(\frac{1}{\Delta T_d} \frac{\Delta T_d}{\ln 2}\right)} \Leftrightarrow \underline{\underline{I_{crit} = e \cdot I_0}} \quad (8)$$

Furthermore, if the result of E^{qn} (7) is put into the right-hand side of E^{qn} (3), the relation of the other parameters in this critical situation can be calculated:

$$\frac{dP_{heat}}{dT_J} = \frac{dP_{cool}}{dT_J} \Rightarrow V_0 \cdot I_0 \cdot 2^{\left(\frac{1}{\Delta T_d} \frac{\Delta T_d}{\ln 2}\right)} \cdot \frac{\ln 2}{\Delta T_d} = \frac{1}{R_{th}} \Leftrightarrow V_0 \cdot I_0 \cdot e \cdot \frac{\ln 2}{\Delta T_d} = \frac{1}{R_{th}} \quad (9)$$

Finally, the criterion for stability reads:

$$\boxed{V_0 \cdot I_0 \cdot R_{th} < \frac{\Delta T_d}{e \cdot \ln 2}} \quad (10)$$

With $\Delta T_d = 11K$:

$$\frac{\Delta T_d}{e \cdot \ln 2} = 5.8K \quad (11)$$

4 Conclusions

Equation (10) gives a simple criterion for stability. The left-hand side includes the main influencing factors: applied voltage V_0, leakage current I_0 at reference temperature and V_0 and thermal resistance, while the right-hand side can be even traced back to basic physics and has a value of **5.8 K** for silicon devices ($\Delta T_d = 11$ K). In any case, this rule of thumb value has to be verified because of unusual contributions to the leakage current or particular device features that can change the temperature dependence significantly. In addition, a safety margin is recommended since homogenous cooling and leakage current over the whole device are assumed which is not realistic in real-world applications.
As shown in the example of Fig. 1, it would be possible to operate the device on a heating plate with $V_0 = 3600$ V and 125 °C if the interface resistance between case and heat-sink were at an acceptably low level. However, it has to be considered, that already in this case, the junction temperature stabilises significantly above 125 °C, influencing the switching characteristics and even the SOA.

In order to characterise the device at $T_{vj} = 125$ °C, one has two options:
- apply V_0 right before the test (e.g. some 100 microsecond) and switch off V_0 directly after the tests have been performed (e.g. some 100 microsecond).
- adjust the heating plate to a lower temperature in order to compensate for the temperature drop across the thermal resistance caused by the expected leakage losses

In all cases, it is crucial to have the lowest possible thermal resistance. Therefore, it is mandatory to mount the module on the heating plate with all screws properly tightened. In addition, thermally conductive grease or at least thermally conductive foil should be used to minimise the thermal resistance of the interface between case and heat-sink and to bring it to the specified (data-sheet) value.
For more detailed information regarding the mounting of HiPak modules please refer to the Technical Note “Mounting Instructions for HiPak Modules” 5SYA 2039.

5 Reference

Nando Kaminski, TN PTS 05-013, Thermal runaway during blocking

6 Revision history

Version	Change	Authors
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